

NSWAA/NTWAA

Liverpool 10

Sunderland 10

LA-5321P REV 1.0 Schematic

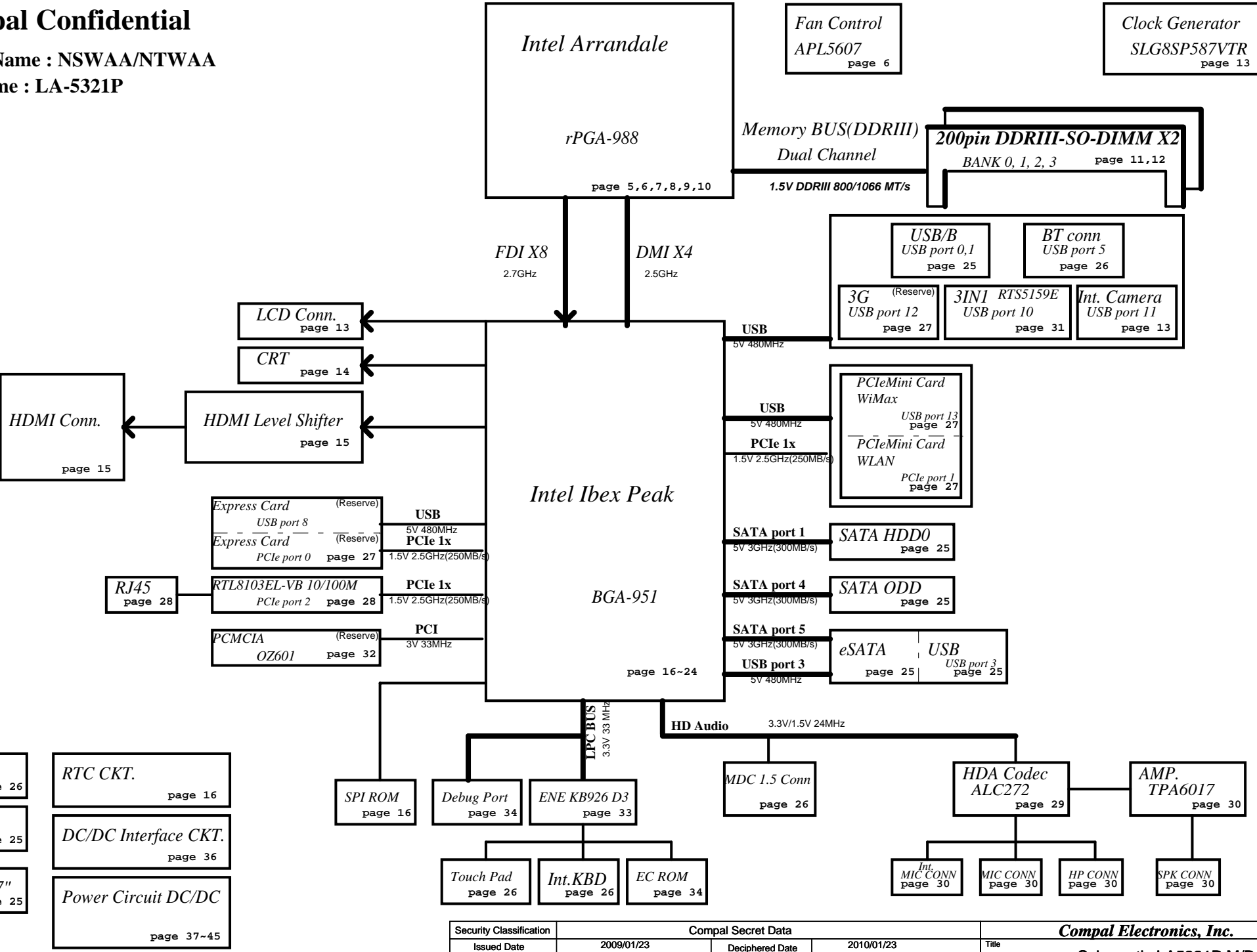
Intel Arrandale /IBEX PEAK

2009-11-12 Rev 1.0

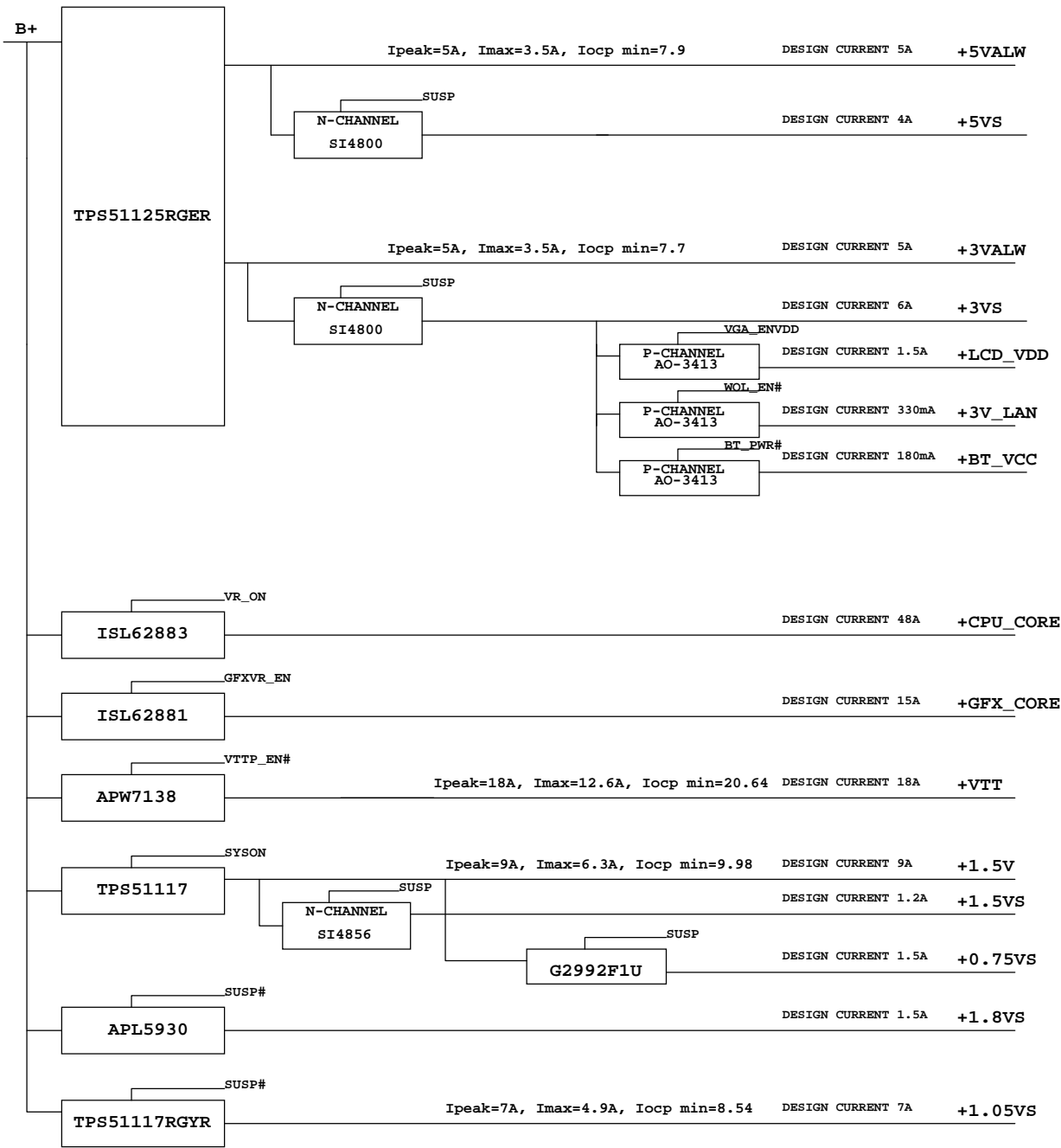
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Compal Confidential

Model Name : NSWAA/NTWAA
File Name : LA-5321P



NSWAA Liverpool Intel Arrandale
NTWAA Sunderland Intel Arrandale



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Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	RJ11	MIC	HDMI	Panel		3G	Express Card		Mini Card
description	(B)			(Y)			(G)	(E)	(A)	
explain	Bluetooth	MDC	MIC	HDMI	16"	17"	3G	New Card	PCMCIA	WIRELESS
BTO	BT@	MDC@	MIC@	IHDMI@	16@	17@	3G@	NEW@	PCM@	WLAN@

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH	HIGH
S3(Suspend to RAM)	LOW	HIGH	HIGH
S4(Suspend to Disk)	LOW	LOW	HIGH
S5(Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

EC SM Bus1 address

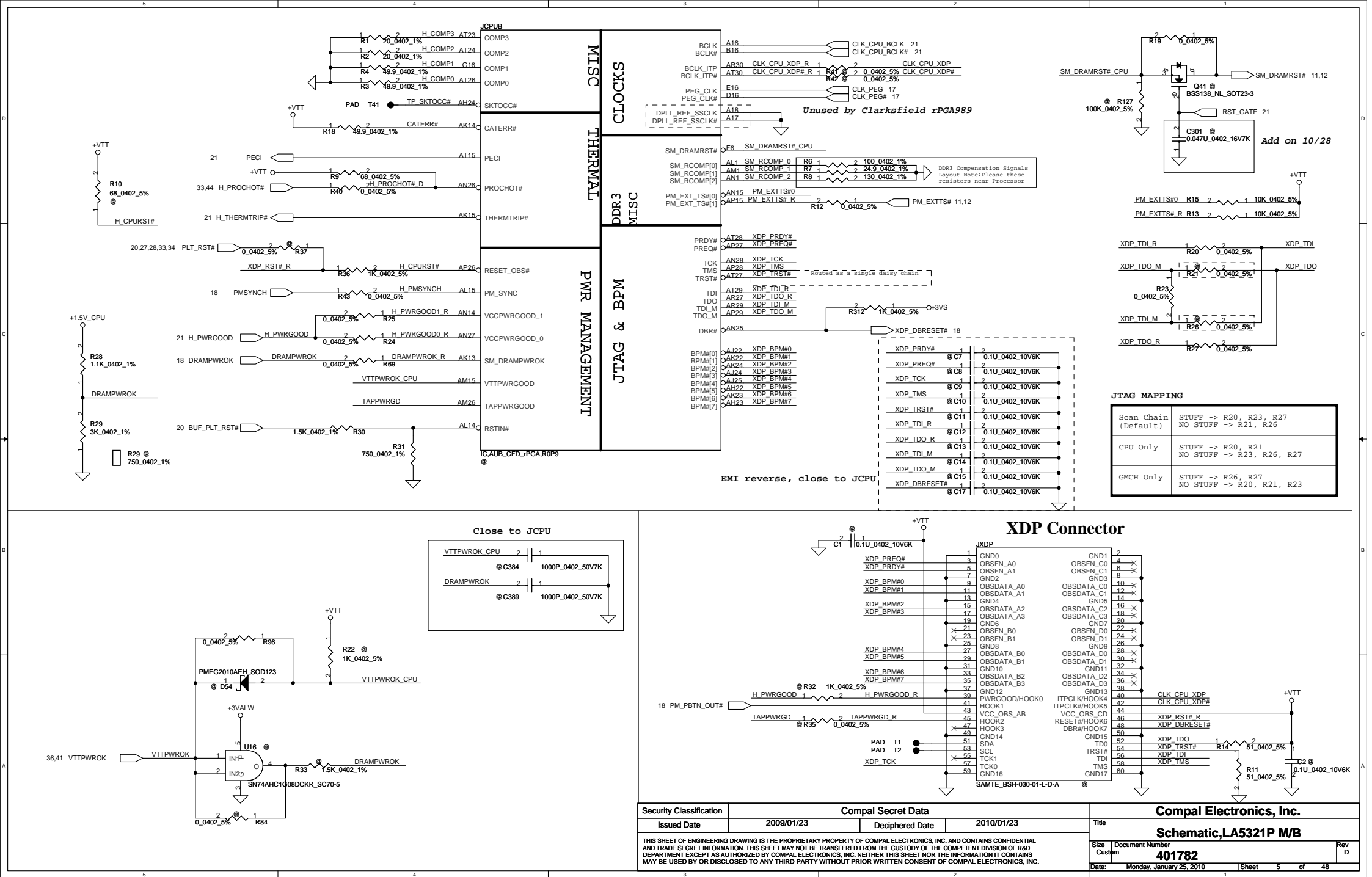
EC SM Bus2 address

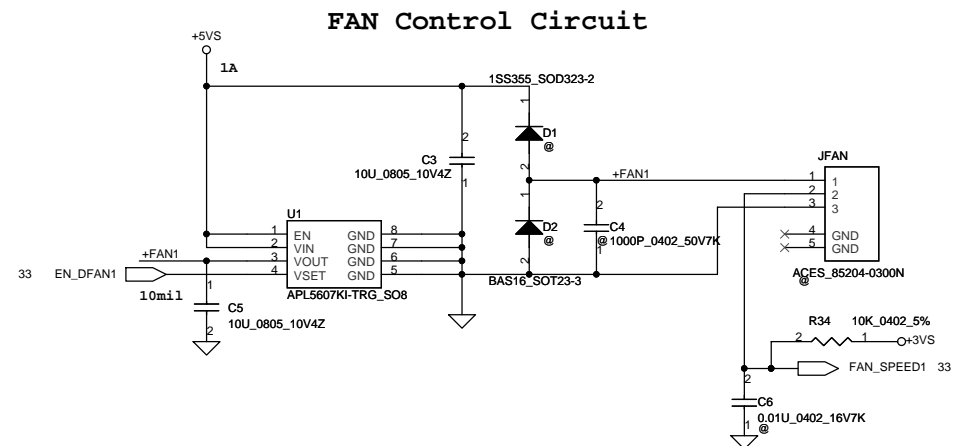
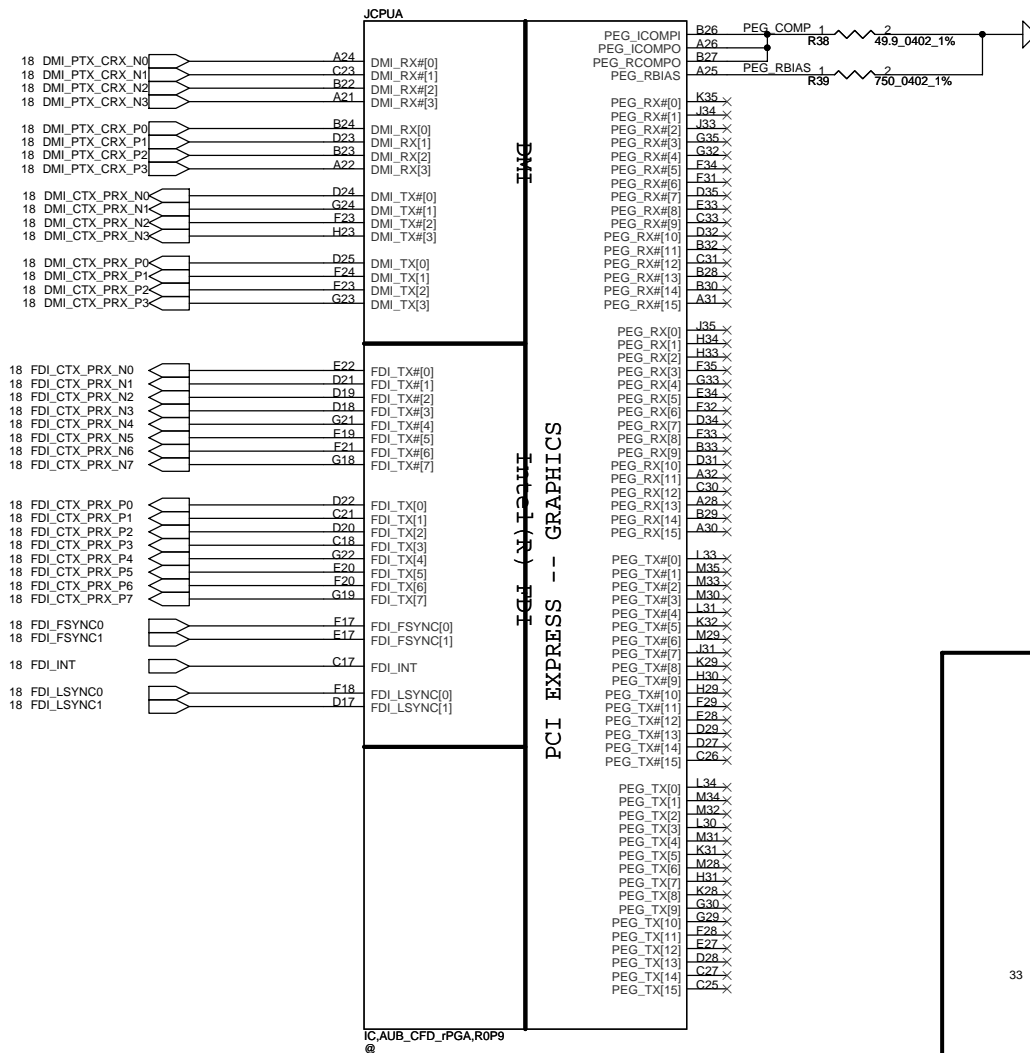
Power	Device	Address	Power	Device	Address
+3VALW	EC KB926 D3		+3VS	EC KB926 D3	
+3VALW	Smart Battery	0001 011x b	+3VS	VGA THM Sensor ADM1032ARMZ	1001 110x b
			+3VS	PCH	0100 110x b

PCH SM Bus address

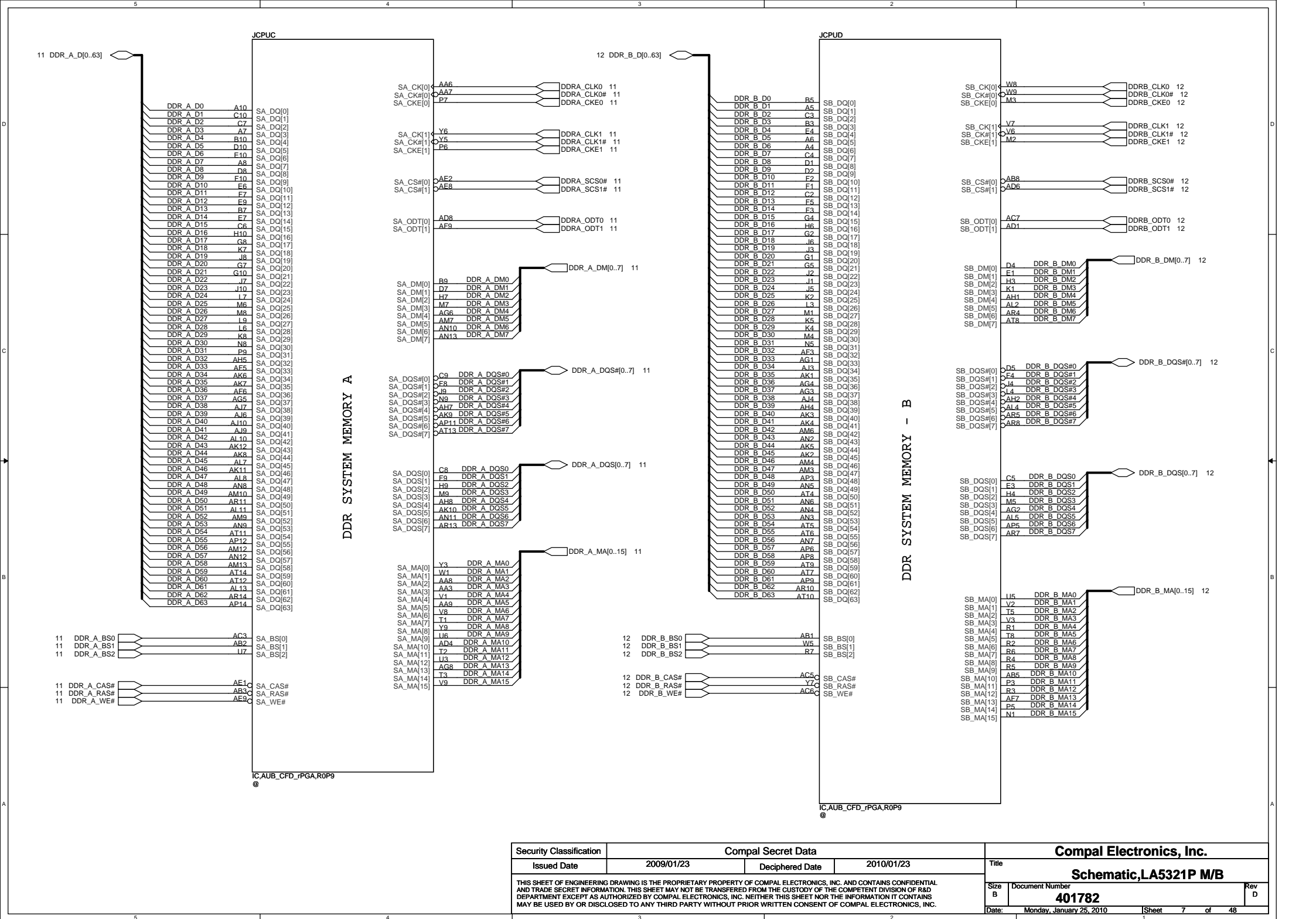
Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	Express	
+3VS	WLAN/Wimax/3G	

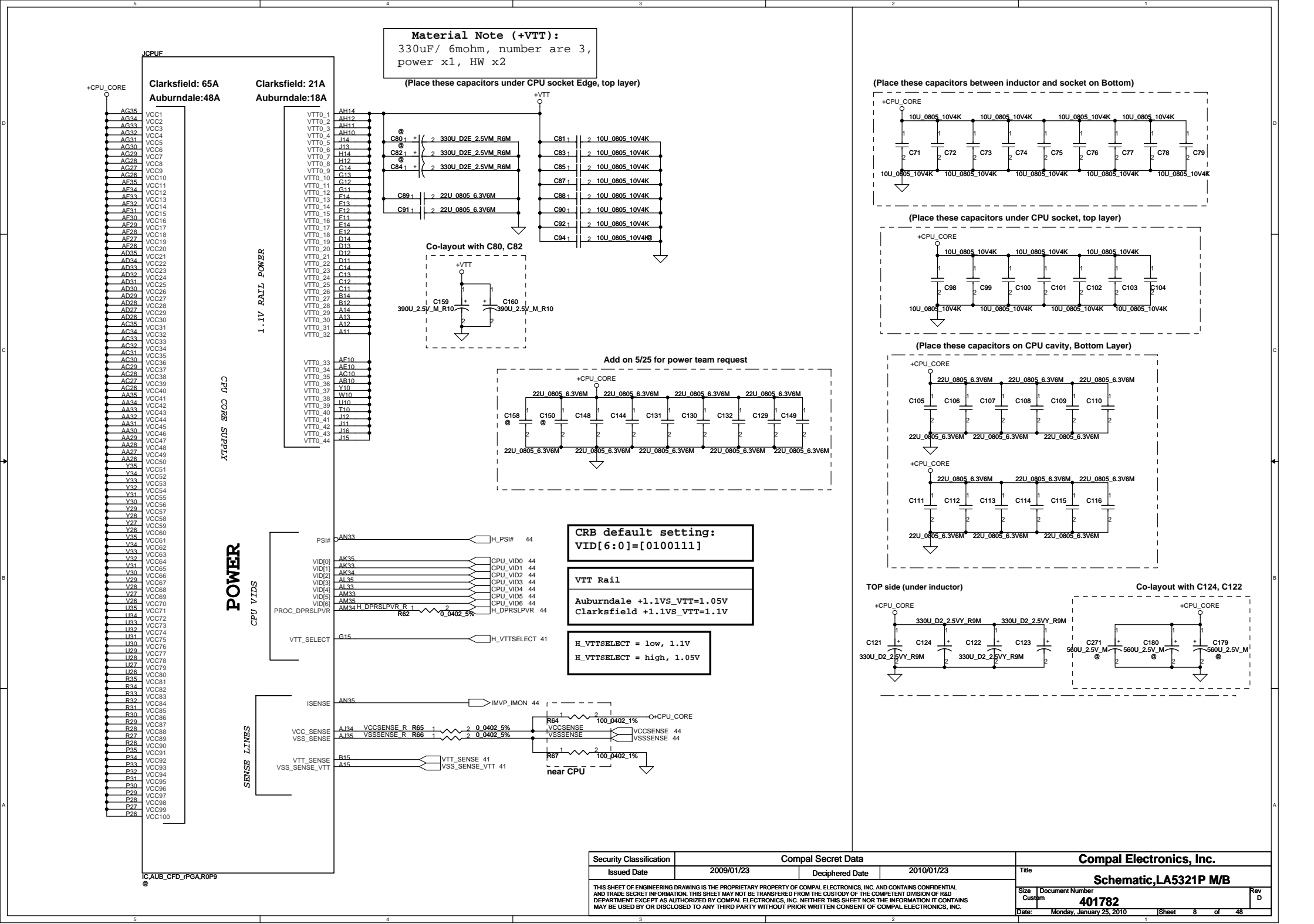
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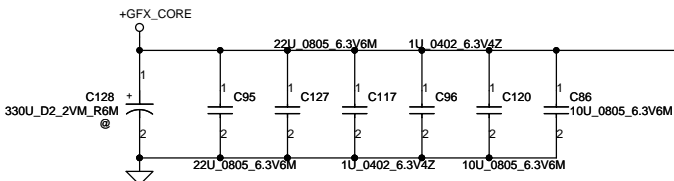
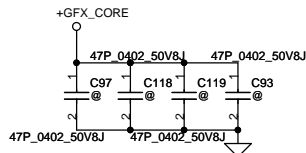




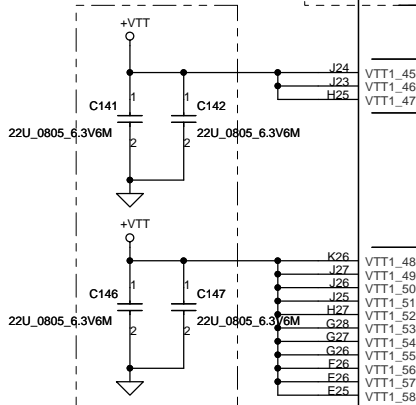
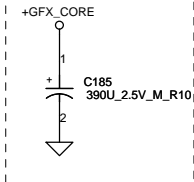
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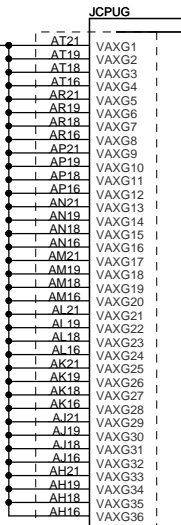




Co-layout with C128



(Place these capacitors under CPU socket, top layer)



GRAPHICS

Clarksfield: 5A
Auburndale: 3A

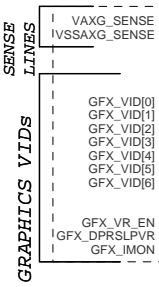
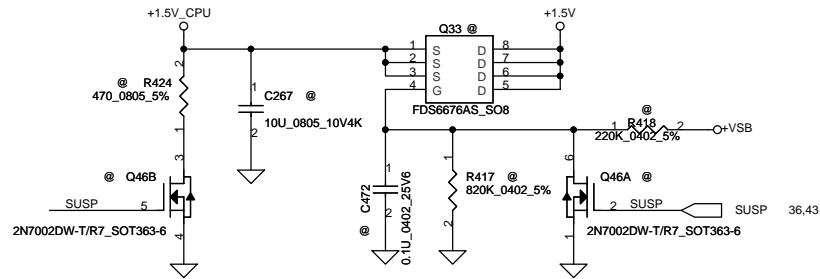
POWER

Clarksfield: 21A
Auburndale: 18A

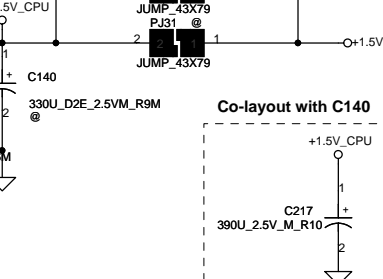
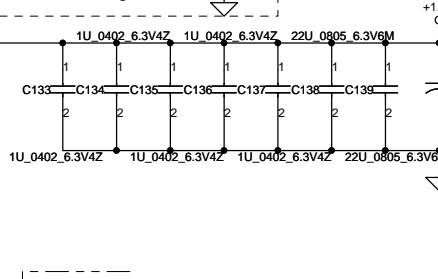
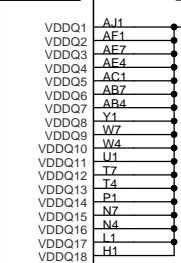
PEG & DMI

Clarksfield: 0.6A
Auburndale: 0.6A

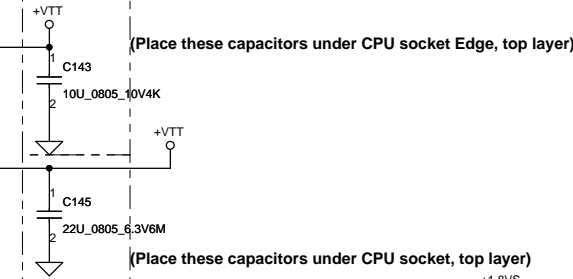
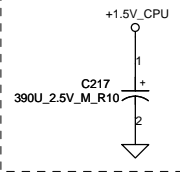
IC:AUB_CFD_rPGA,R0P9



DDR3 - 1.5V RAILS

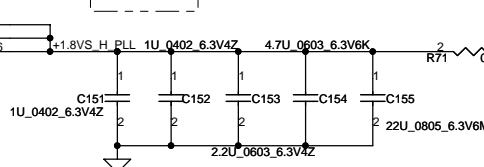


Co-layout with C140

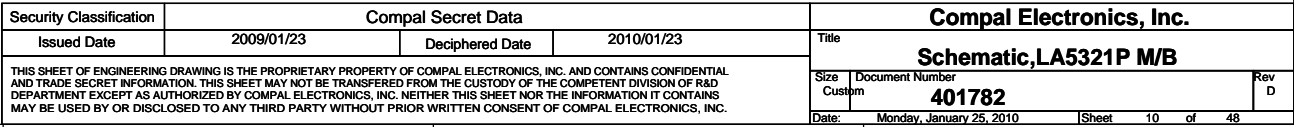


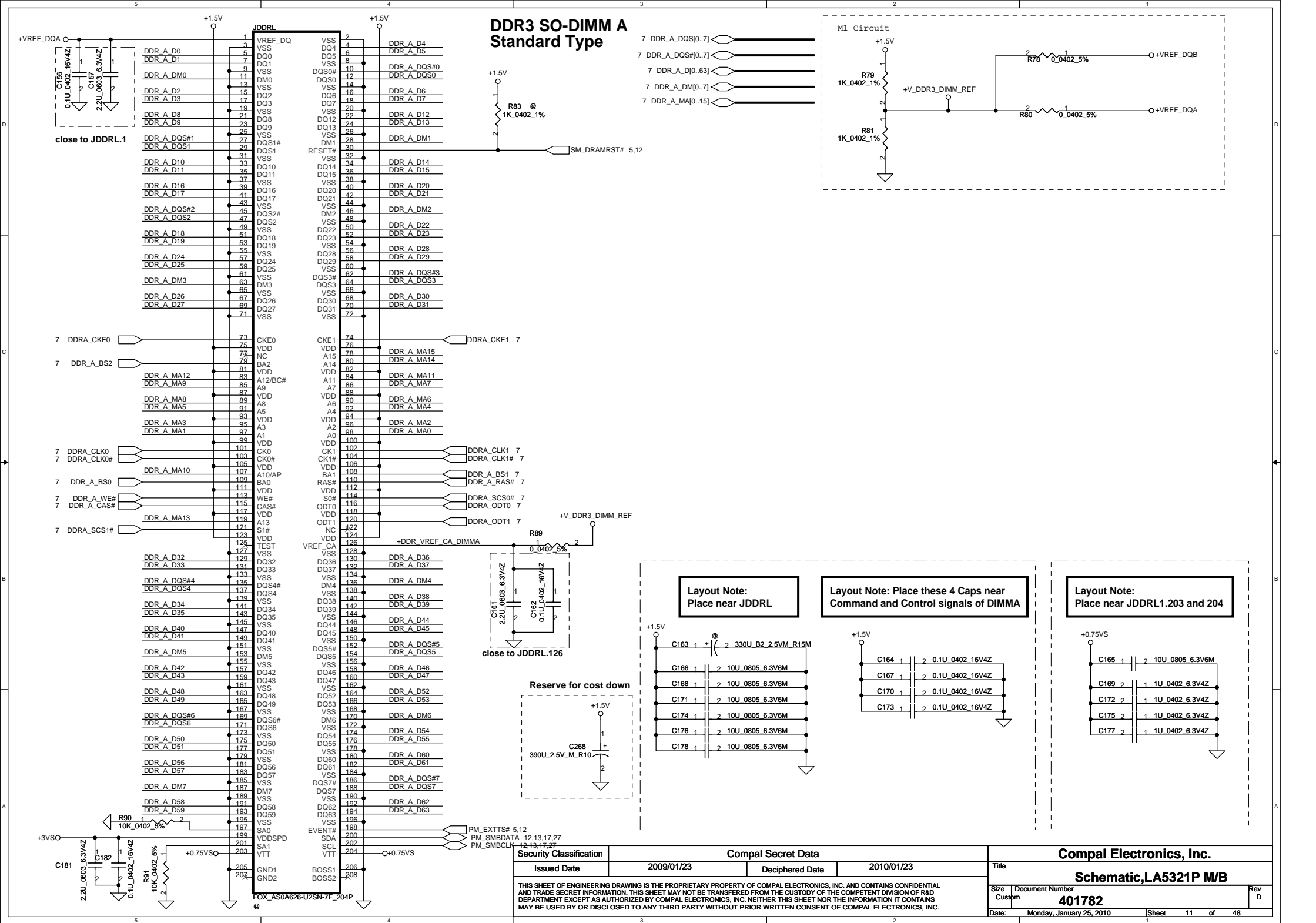
(Place these capacitors under CPU socket Edge, top layer)

(Place these capacitors under CPU socket, top layer)

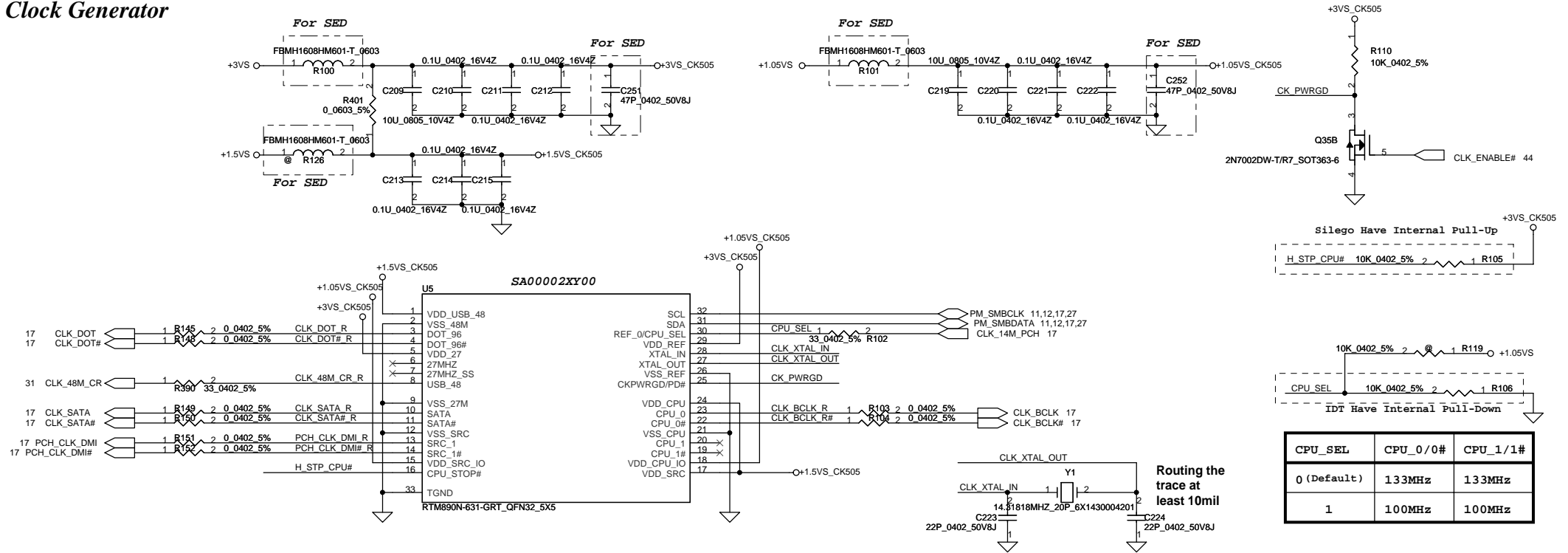


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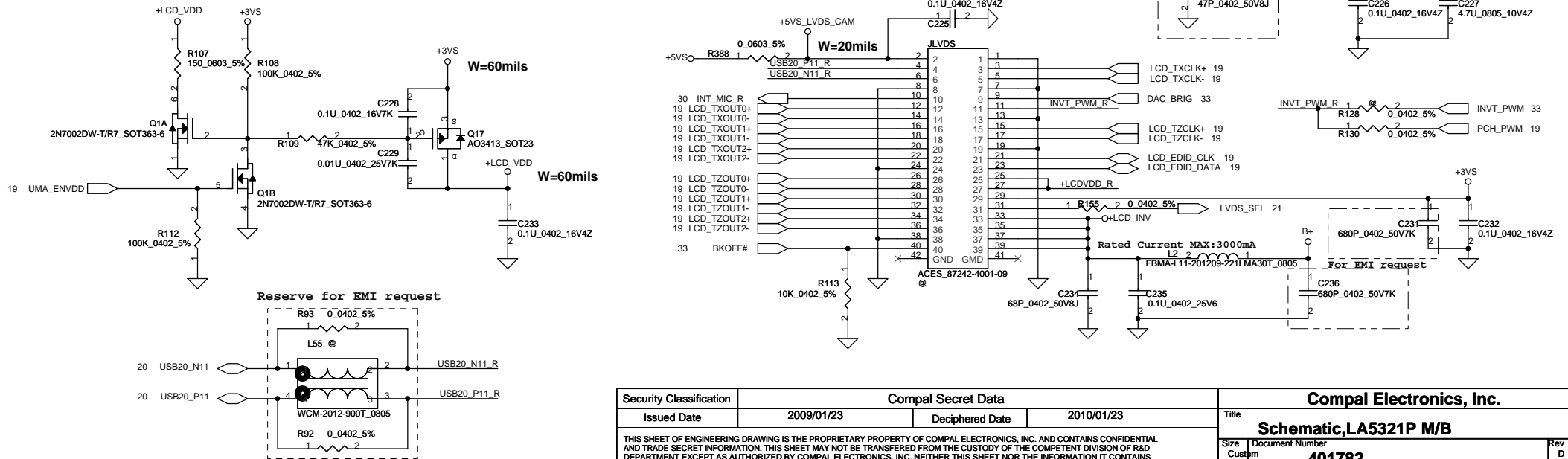




Clock Generator

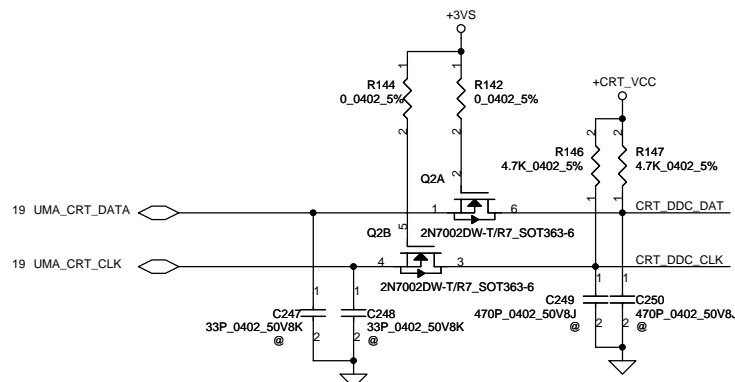
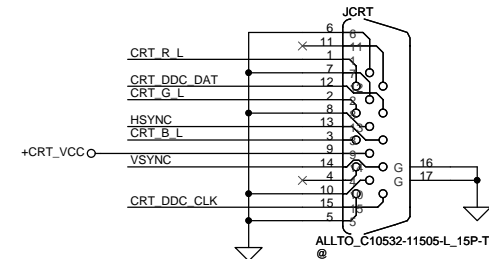
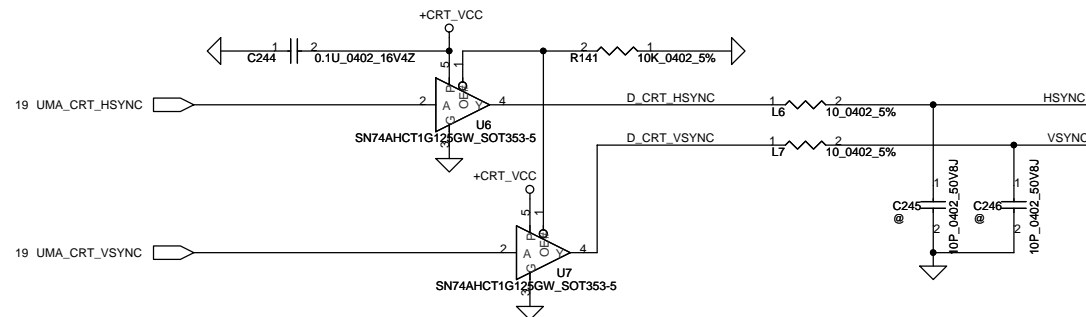
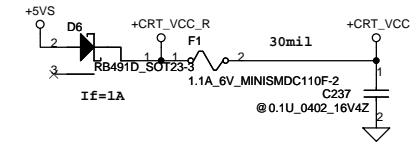
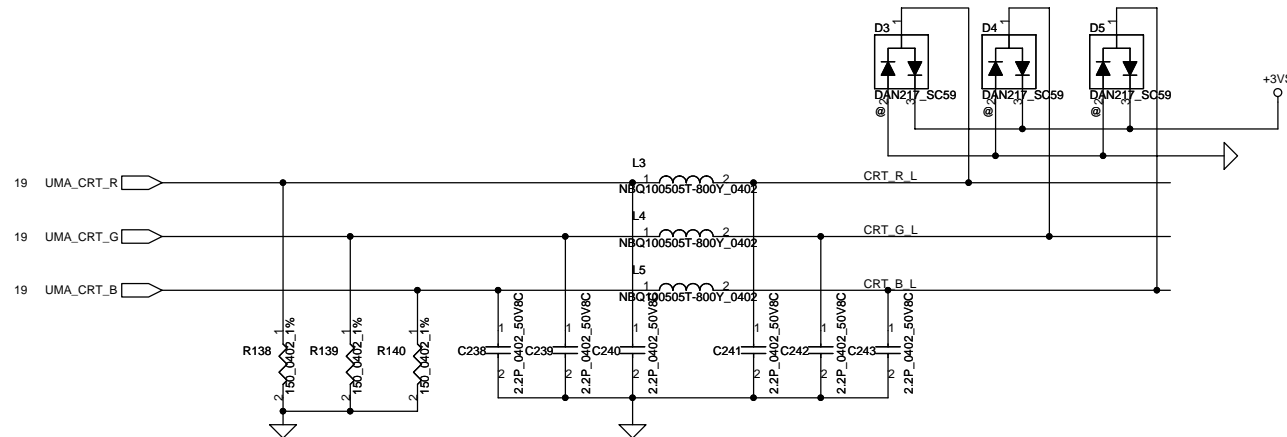


LCD/PANEL BD. Conn.

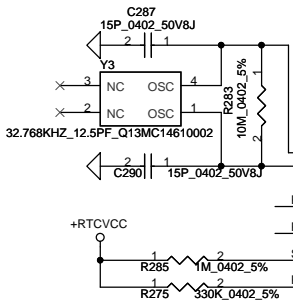
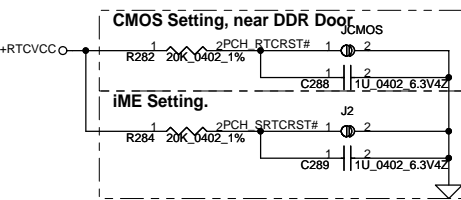


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CRT CONNECTOR



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Integrated SUS 1.05V VRM Enable	
PCH_INTVRMEN	High - Enable Internal VRs (must be always pulled high)

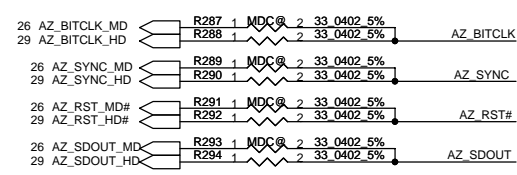
HDA_SYNC

This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

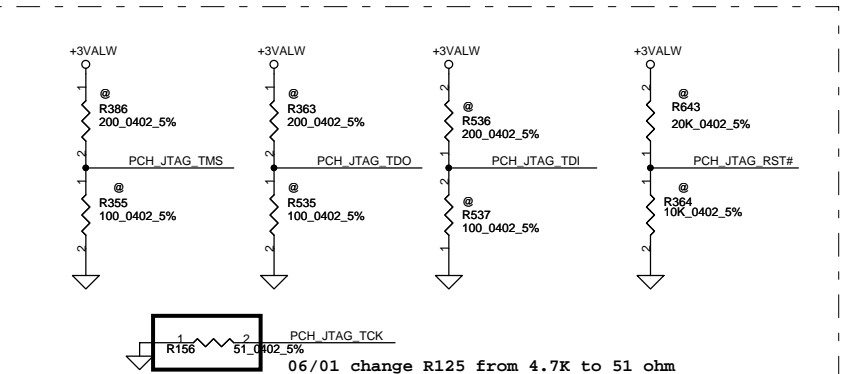
HDA_SDO

This signal has a weak internal pull down.
This signal can't PU

Flash Descriptor Security Override	
HDA_DOCK_EN#	Low = Enabled High = Disabled *

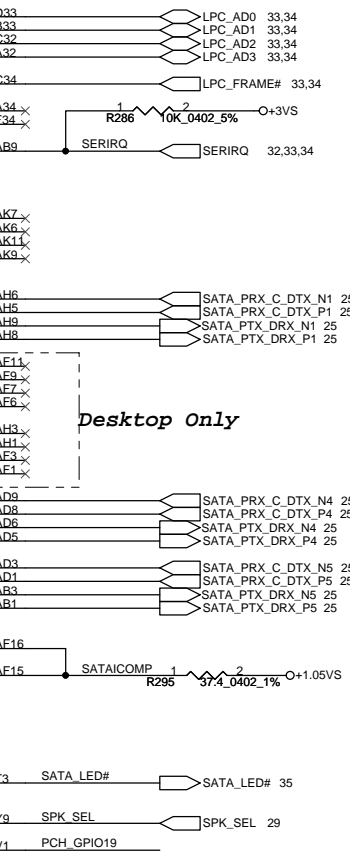
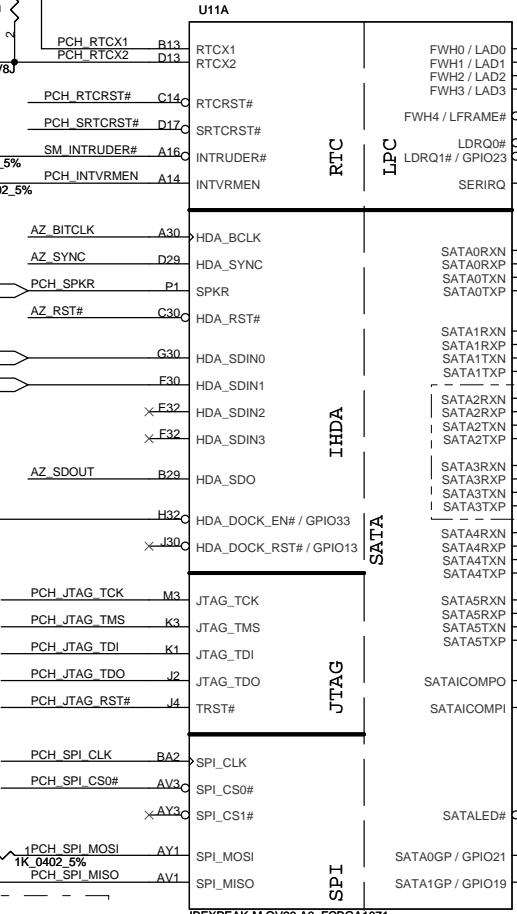


ITPM Enabled Internal: Pull down 20k	
SPI_MOSI	High = Enabled Low = Disabled (Default)



PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
PCH_JTAG_TMS	R355	No Install	100ohm	No Install	No Install
PCH_JTAG_TDI	R354	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDO	R356	200ohm	200ohm	20Kohm	No Install
PCH_JTAG_TDI	R537	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R643	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_RST#	R353	10Kohm	10Kohm	No Install	No Install

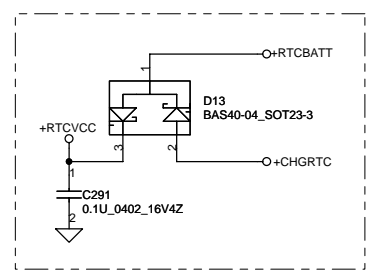
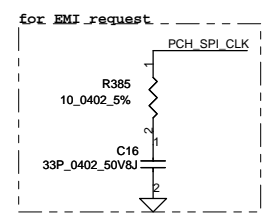
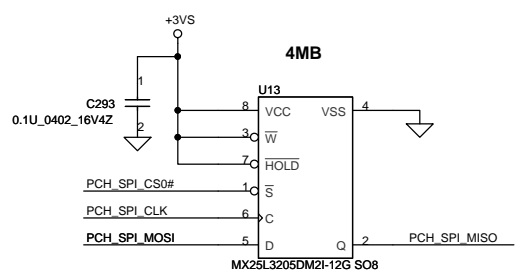
06/01 change R125 from 4.7K to 51 ohm



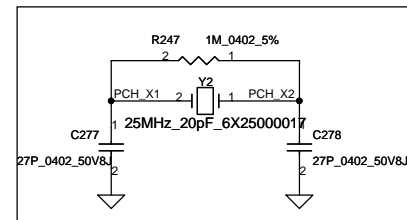
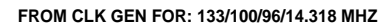
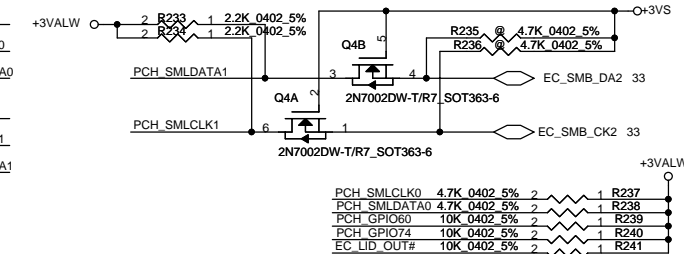
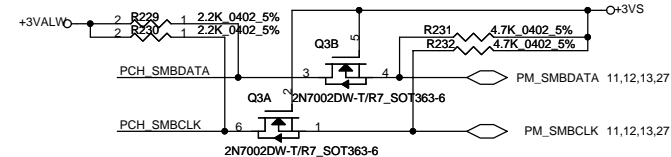
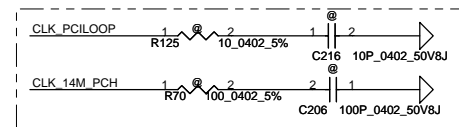
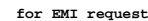
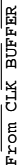
1ST HDD


SATA ODD

eSATA



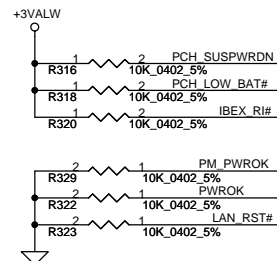
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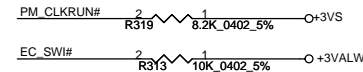
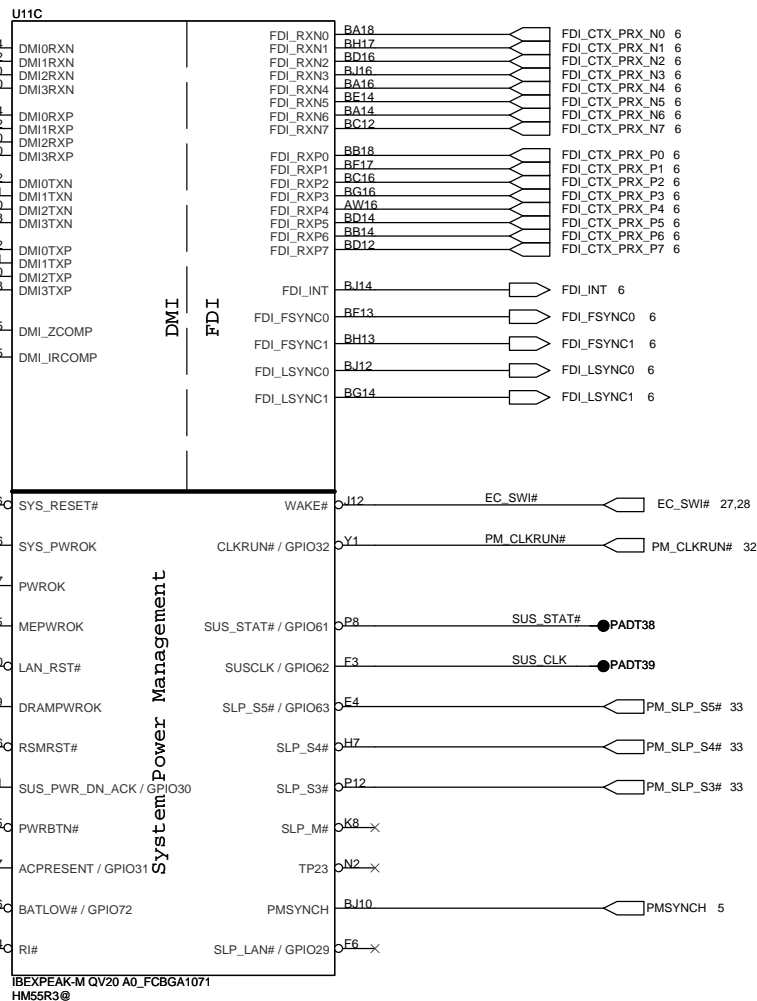
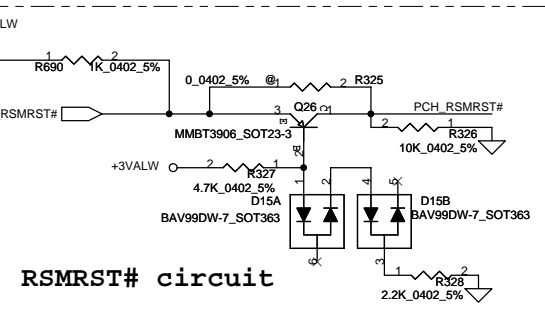
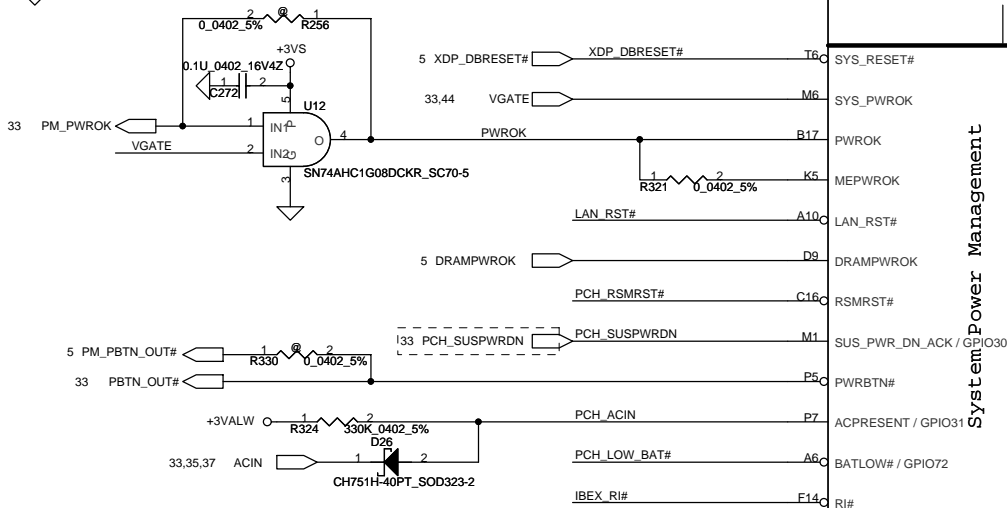
 C277 @
0_0402_5%

Note: Stuff 0 ohm if
25MHz crystal un-stuff

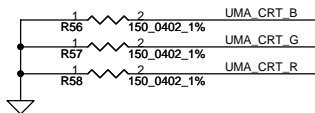
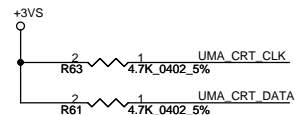
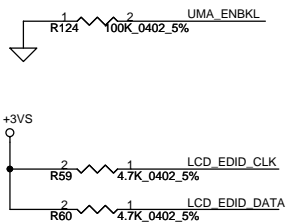
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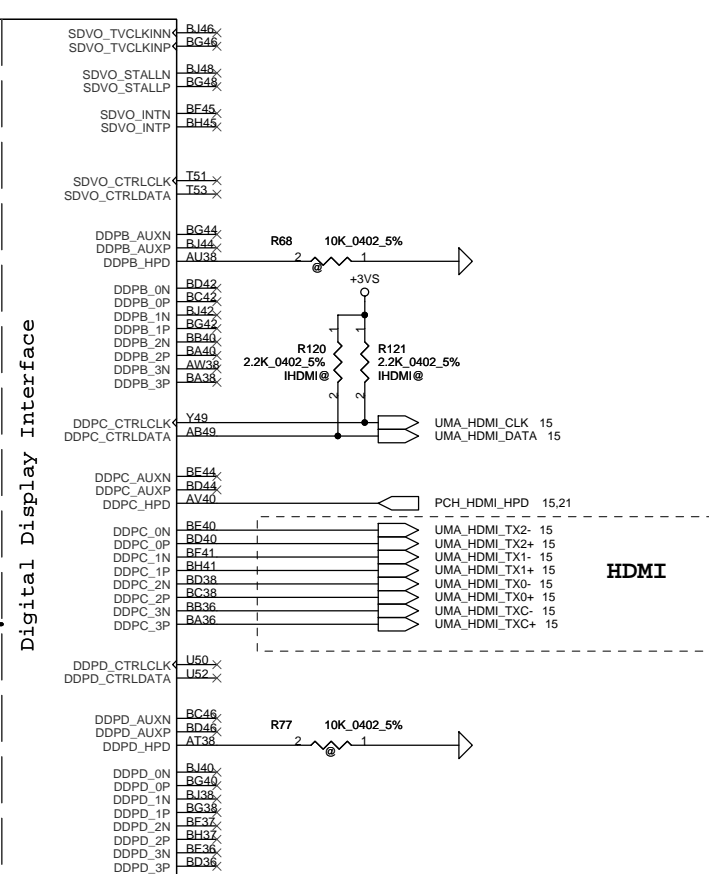
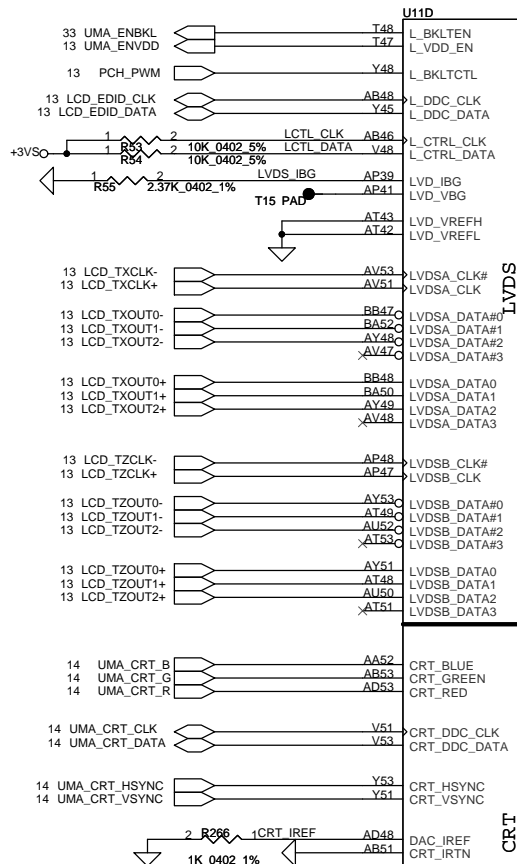
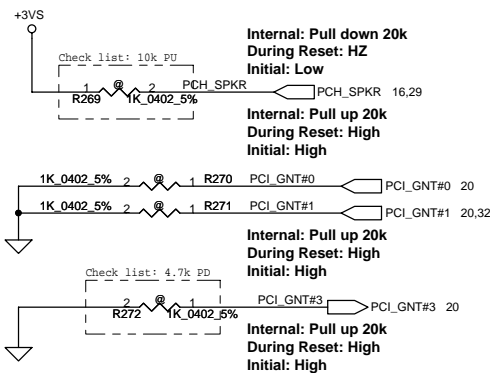
Close to PCH



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Size B	Document Number	401782		Rev D	
Date:	Monday, January 25, 2010	Sheet	18	of	48



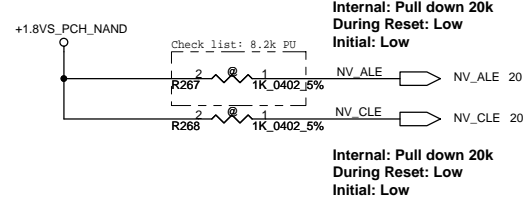
PCH Strap Pin



NO REBOOT Strap		
PCH_SPKR	Low= Disable High= Enable	

Boot BIOS Strap		
PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

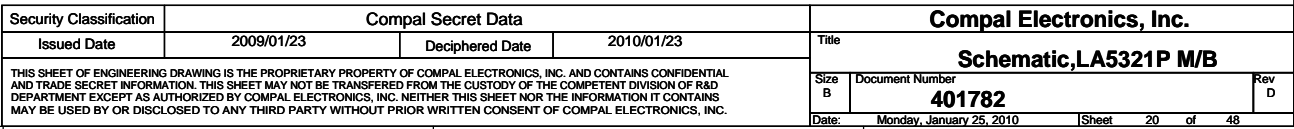
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable

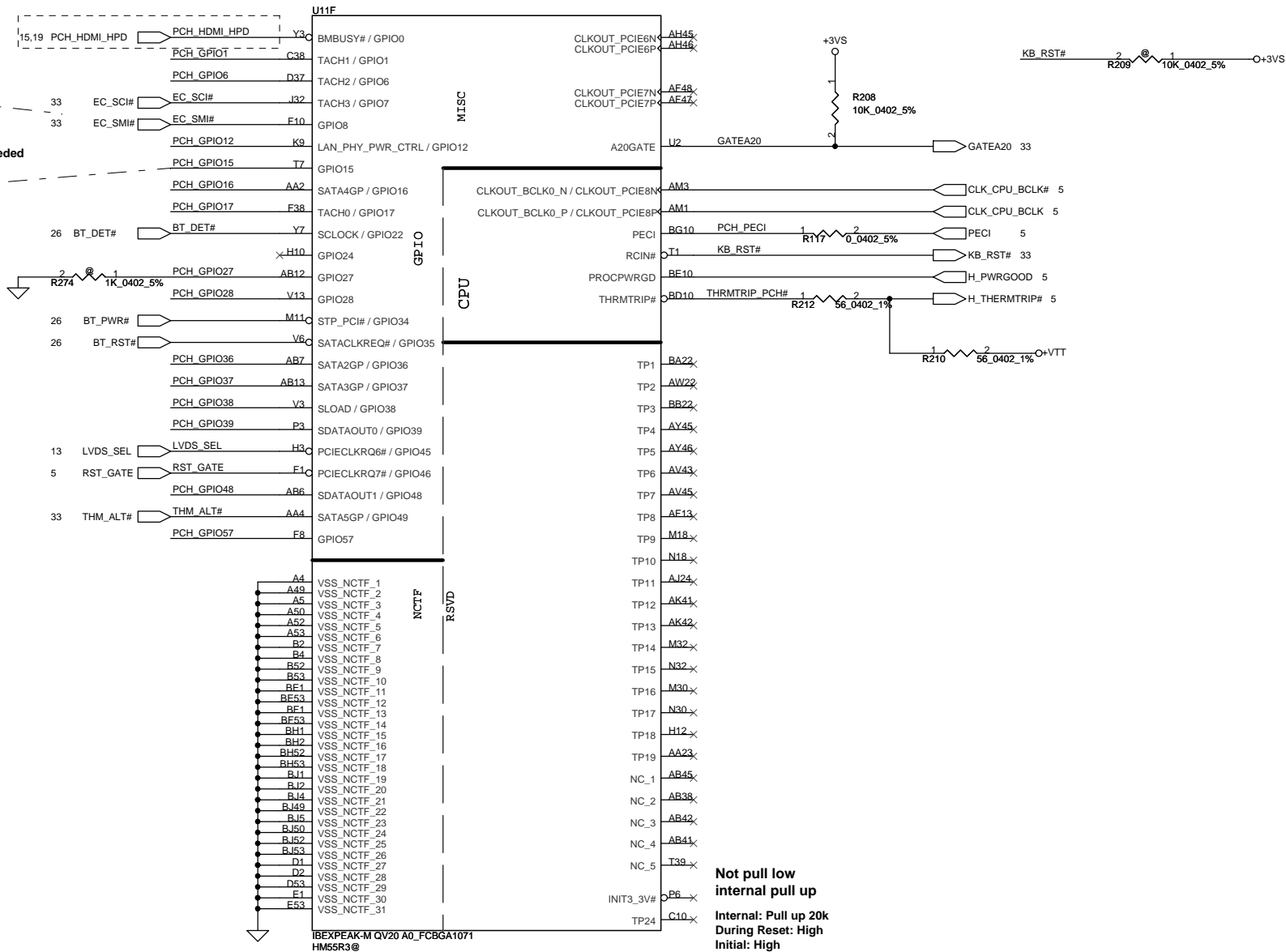
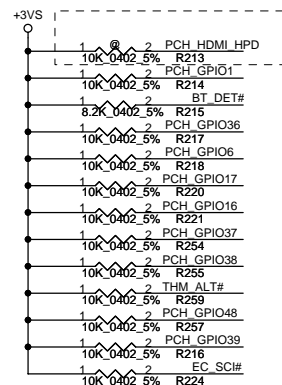
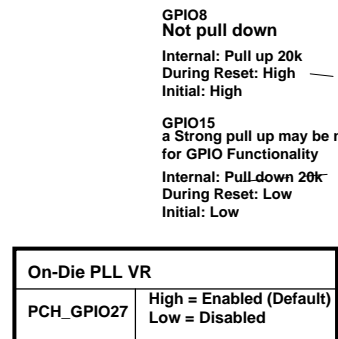


Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled (Default)

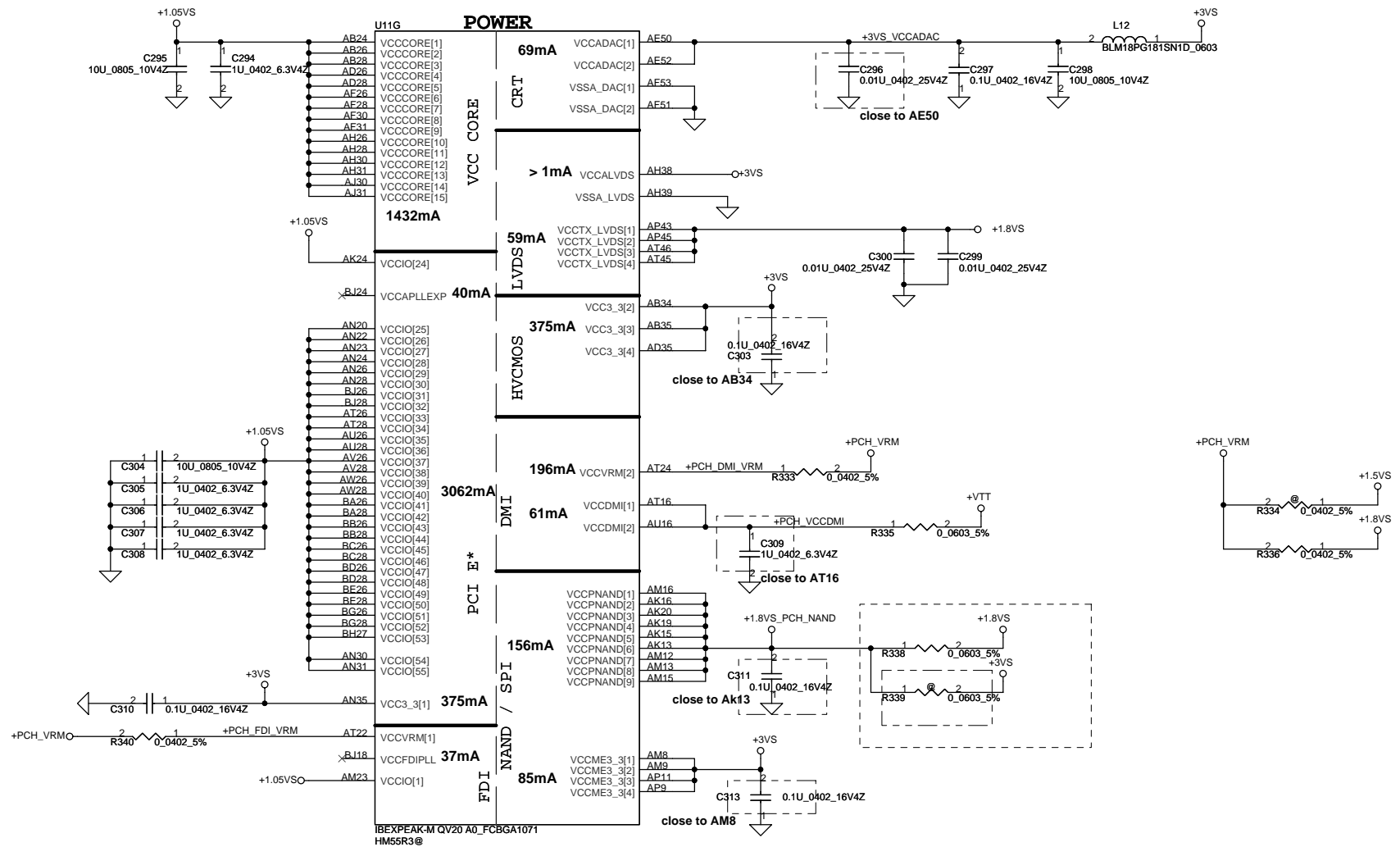
DMI Termination Voltage	
NV_CLE	Low= Set to Vss (Default) High= Set to Vcc

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				Date: Monday, January 25, 2010	Rev D



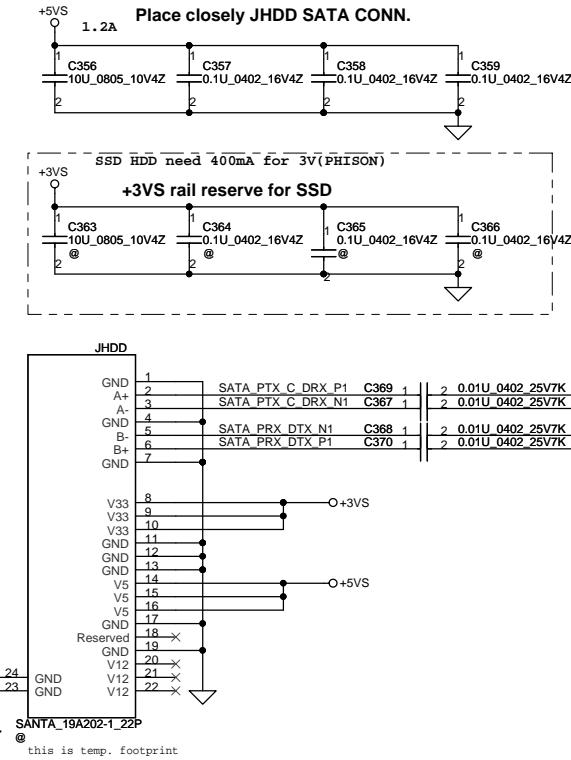


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				B	401782	D
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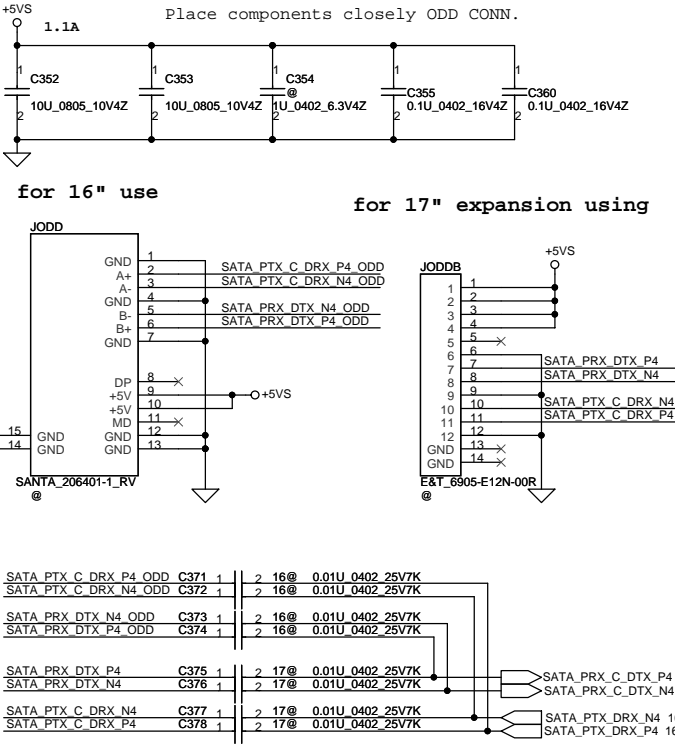


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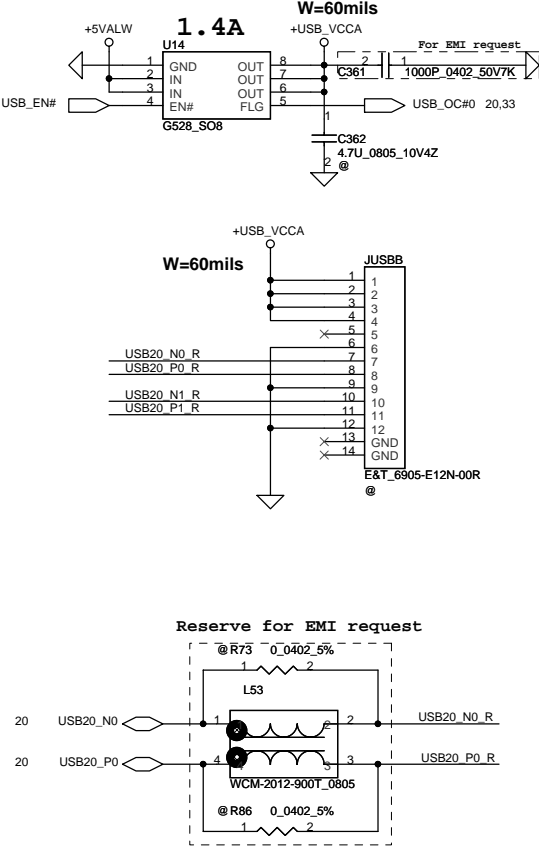
SATA HDD Conn.



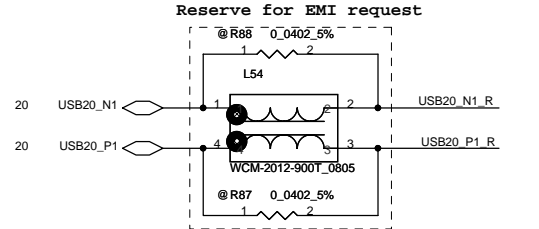
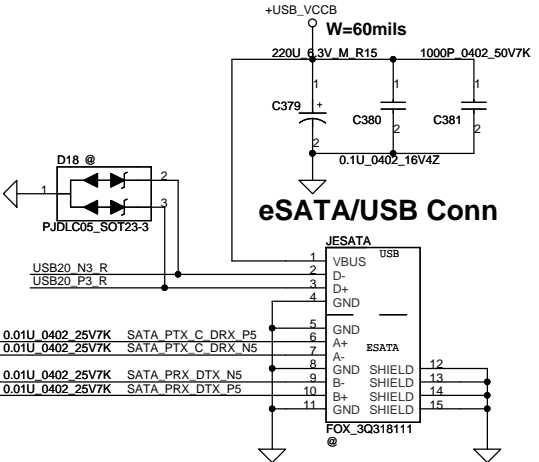
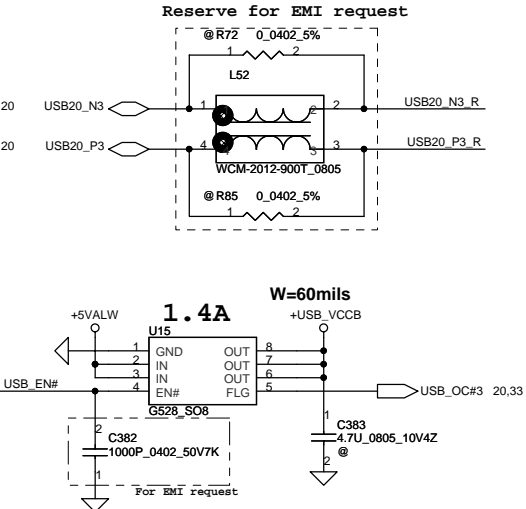
SATA ODD Conn



USB Board

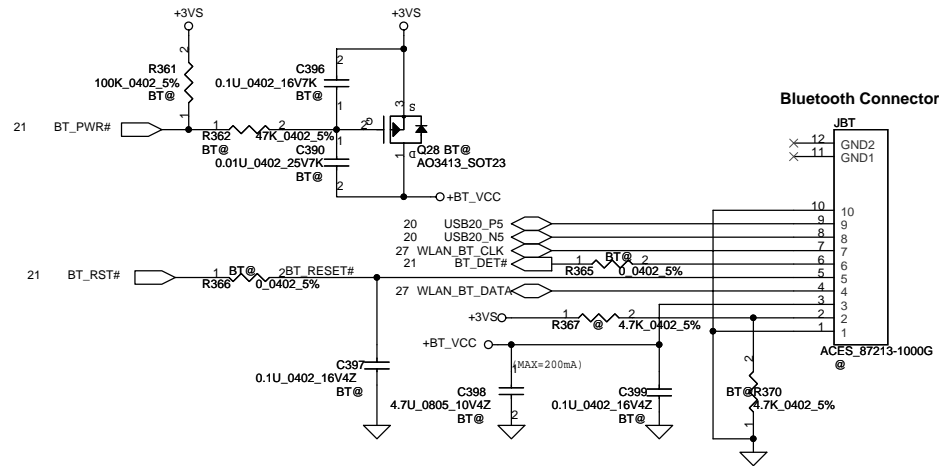


eSATA/USB

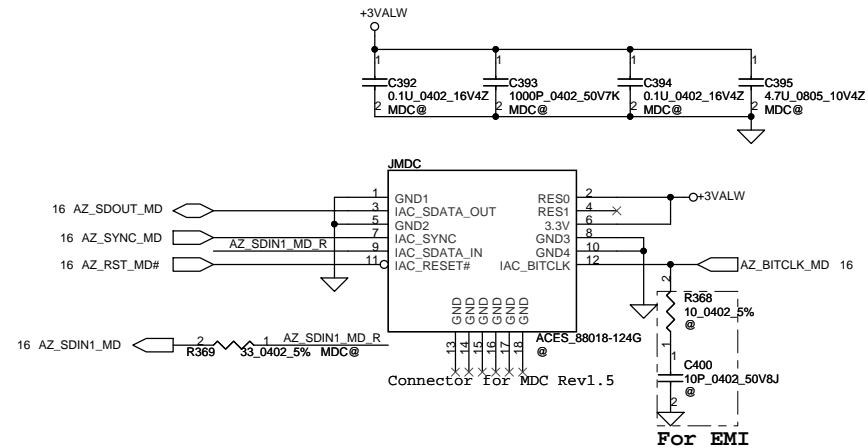


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BlueTooth Interface

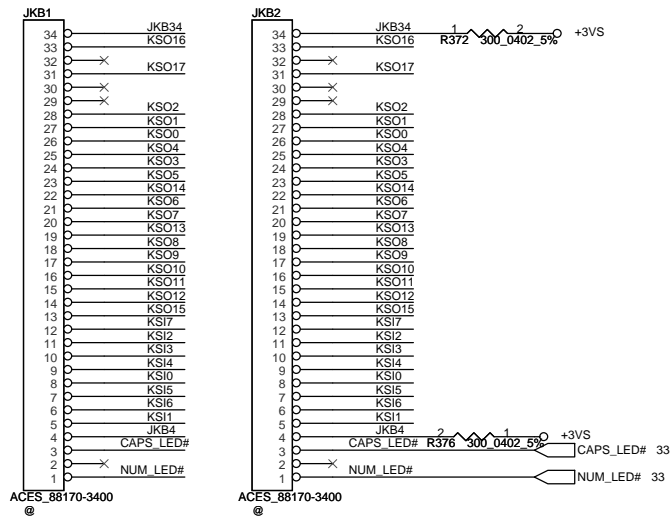


MDC 1.5 Conn.



KEYBOARD CONN. for 16" KEYBOARD CONN. for 17"

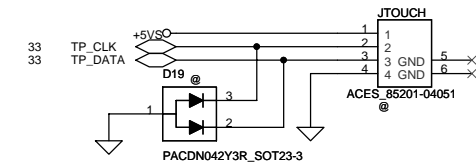
KS[0..7] KS[0..7] 33
KSQ[0..17] KSQ[0..17] 33



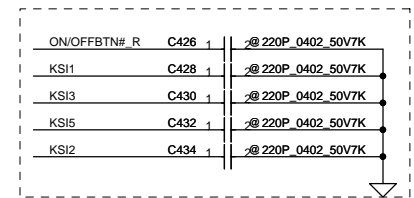
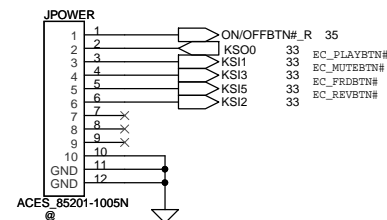
please close to JKB1

KSO16	1	2
KSO17	1	2
KSO2	1	2
KSO1	1	2
KSO0	1	2
KSO4	1	2
KSO3	1	2
KSO5	1	2
KSO14	1	2
KSO6	1	2
KSO7	1	2
KSO13	1	2
KSO8	1	2
KSO9	1	2
KSO10	1	2
KSO11	1	2
KSO12	1	2
KSO15	1	2
KSI7	1	2
KSI2	1	2
KSI3	1	2
KSI4	1	2
KSI5	1	2
KSI6	1	2
KSI1	1	2
KJB4	1	2
CAPS_LED#	1	2
NUM_LED#	1	2

Touch/B Connector



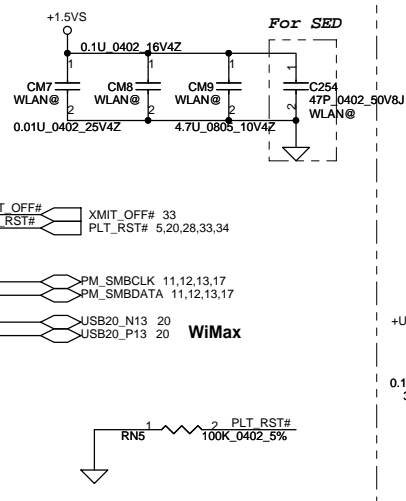
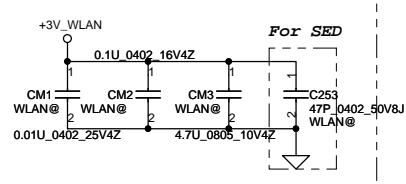
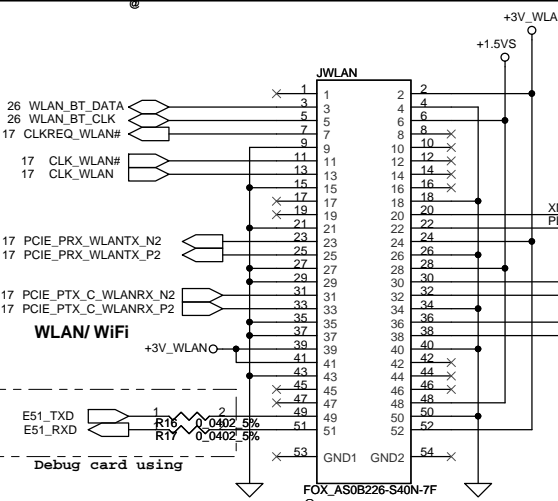
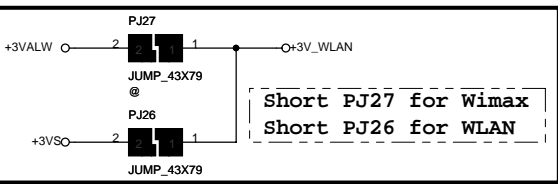
SW/B Connector



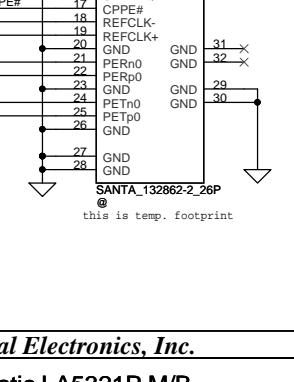
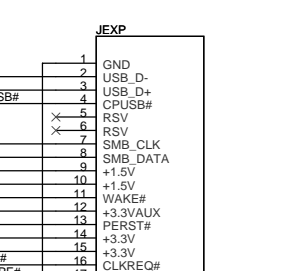
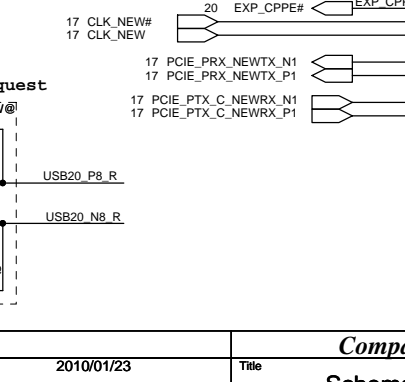
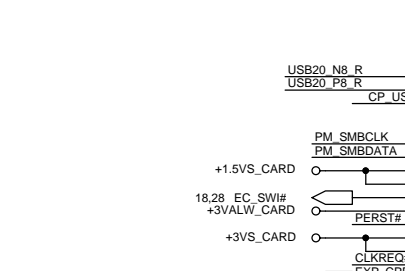
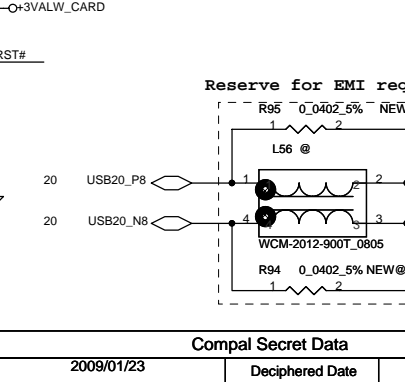
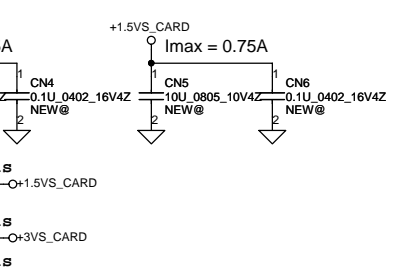
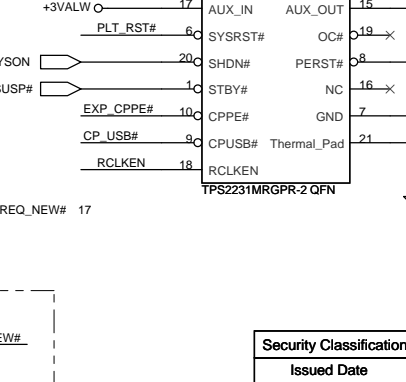
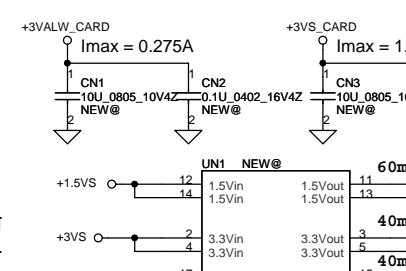
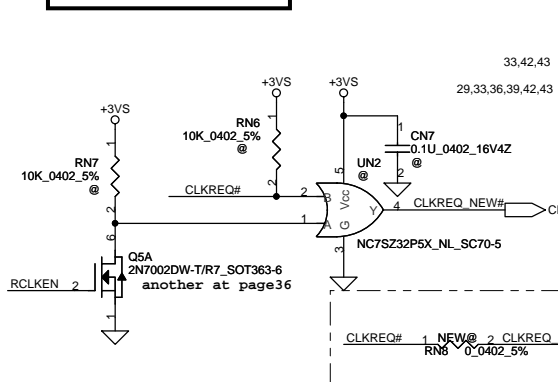
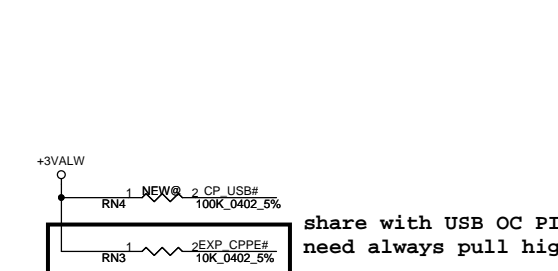
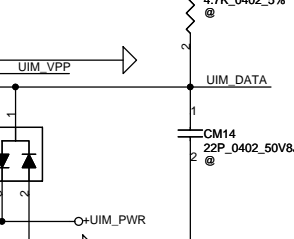
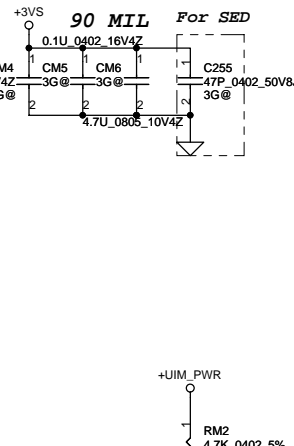
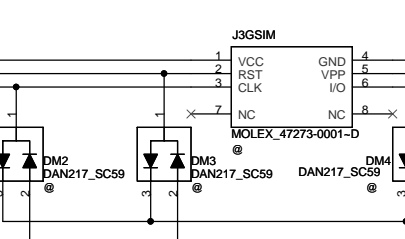
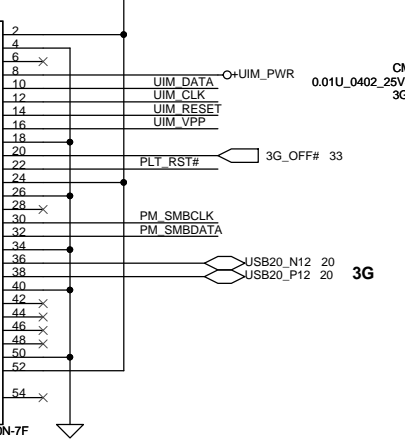
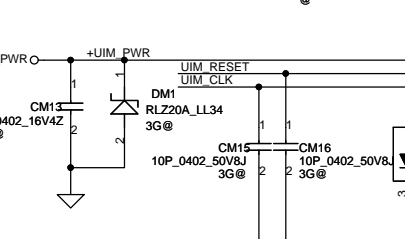
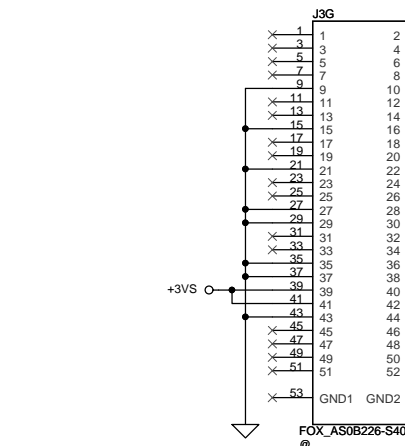
For EMI

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PCIe Mini Card-WLAN/WiMax

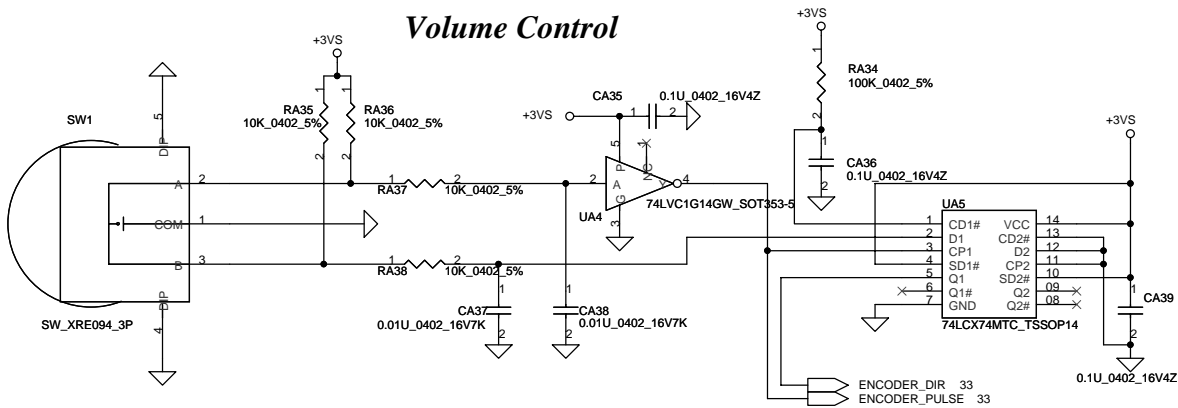
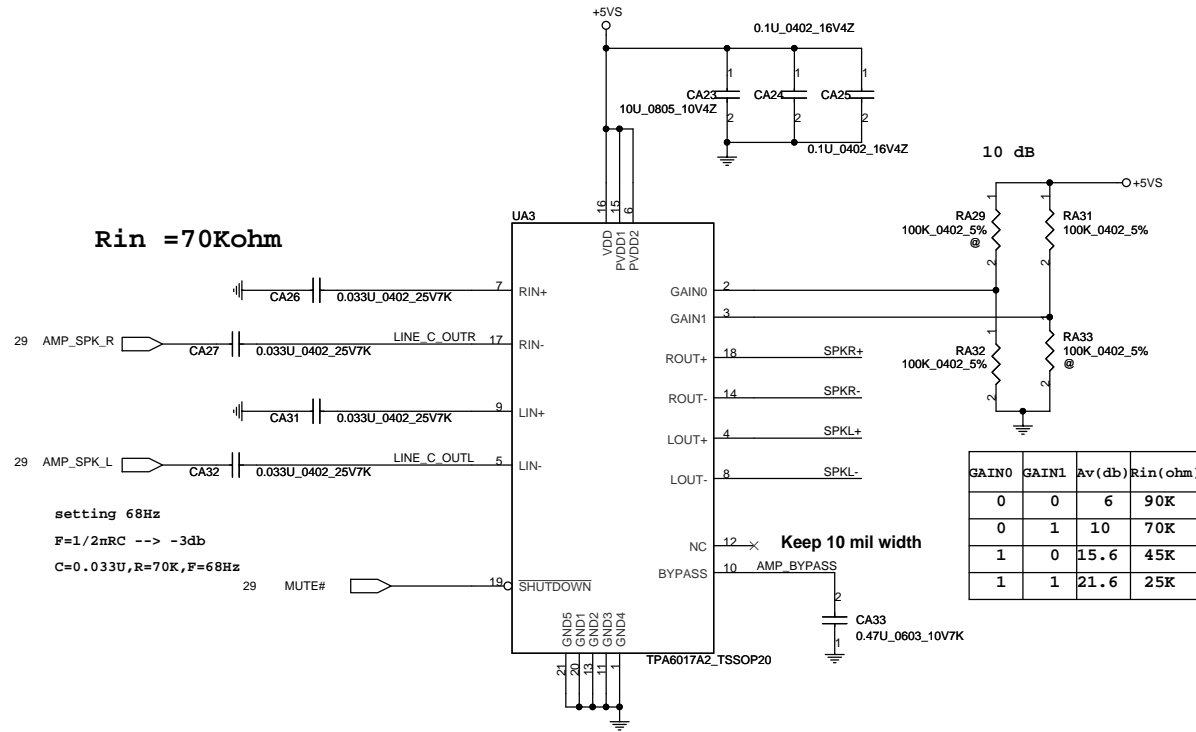


PCIe Mini Card-3G

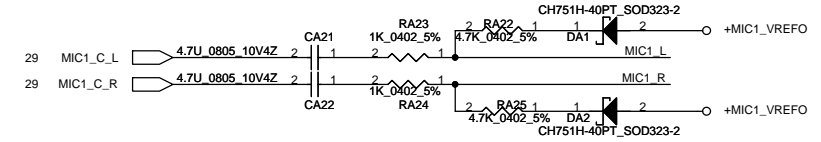


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						Date:		Monday, January 25, 2010		Sheet 27 of 48	

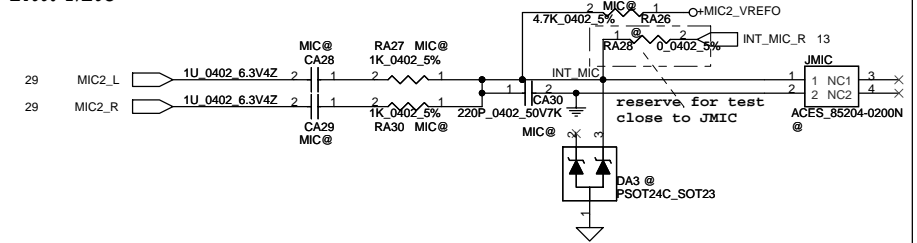
TPA6017 Medium Range Amplifier



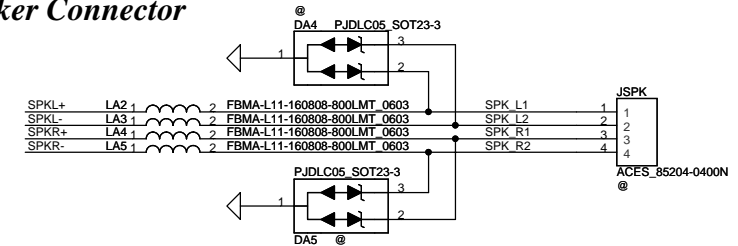
Ext. Mic



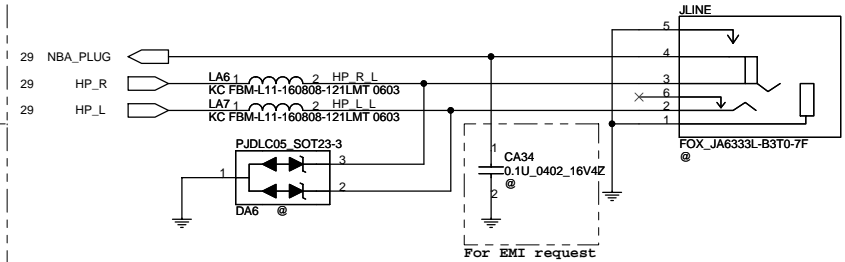
Int. Mic



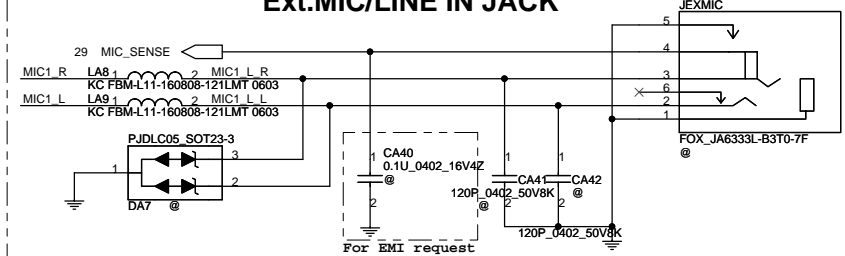
Speaker Connector



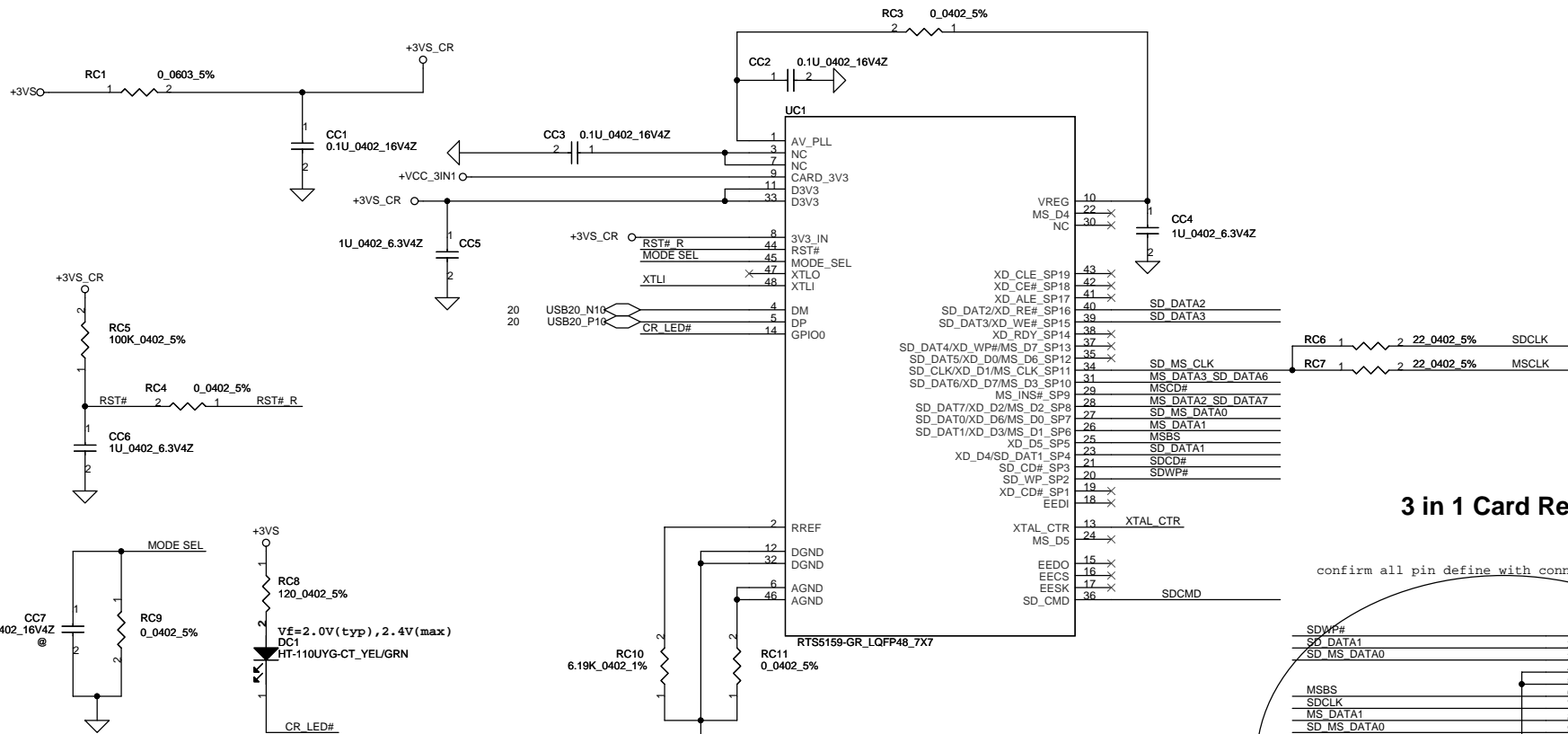
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

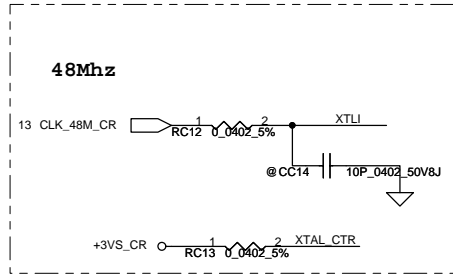
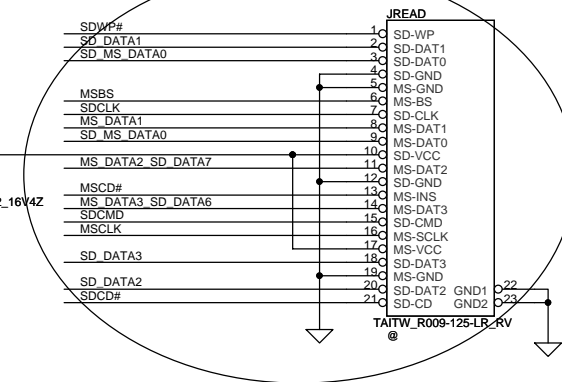


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Size		Document Number		Rev D
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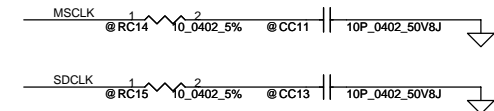


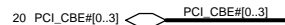
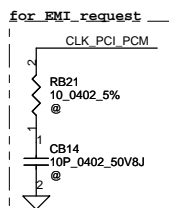
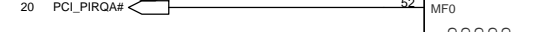
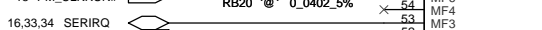
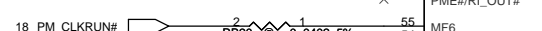
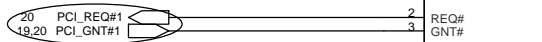
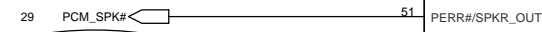
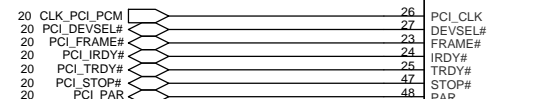
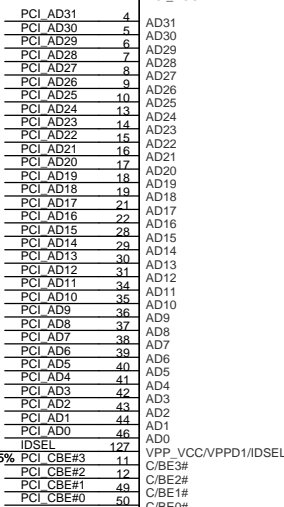
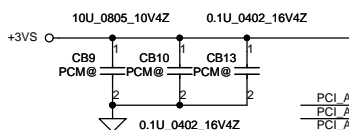
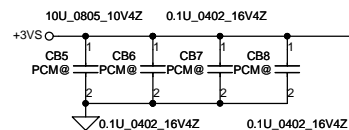
3 in 1 Card Reader

confirm all pin define with connector spec.

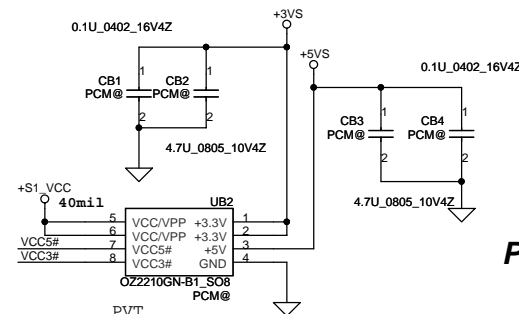
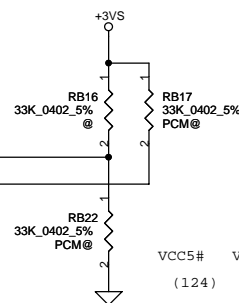


R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

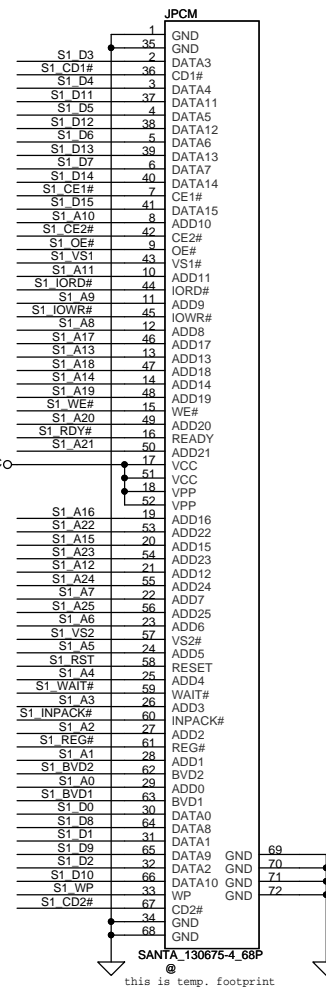


IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#. PME#. SERIRO# & CLKRUN#.



PCMCIA Socket



✓ this is temp. footprint

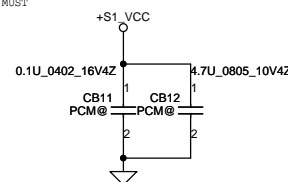
VCC5# (124)	VPP_PGM (125)	IDSEL SELECT
0	0	AD18
0	1	★AD20
1	0	AD25
1	1	PIN F4

NOTE: IDSEL SELECTION!

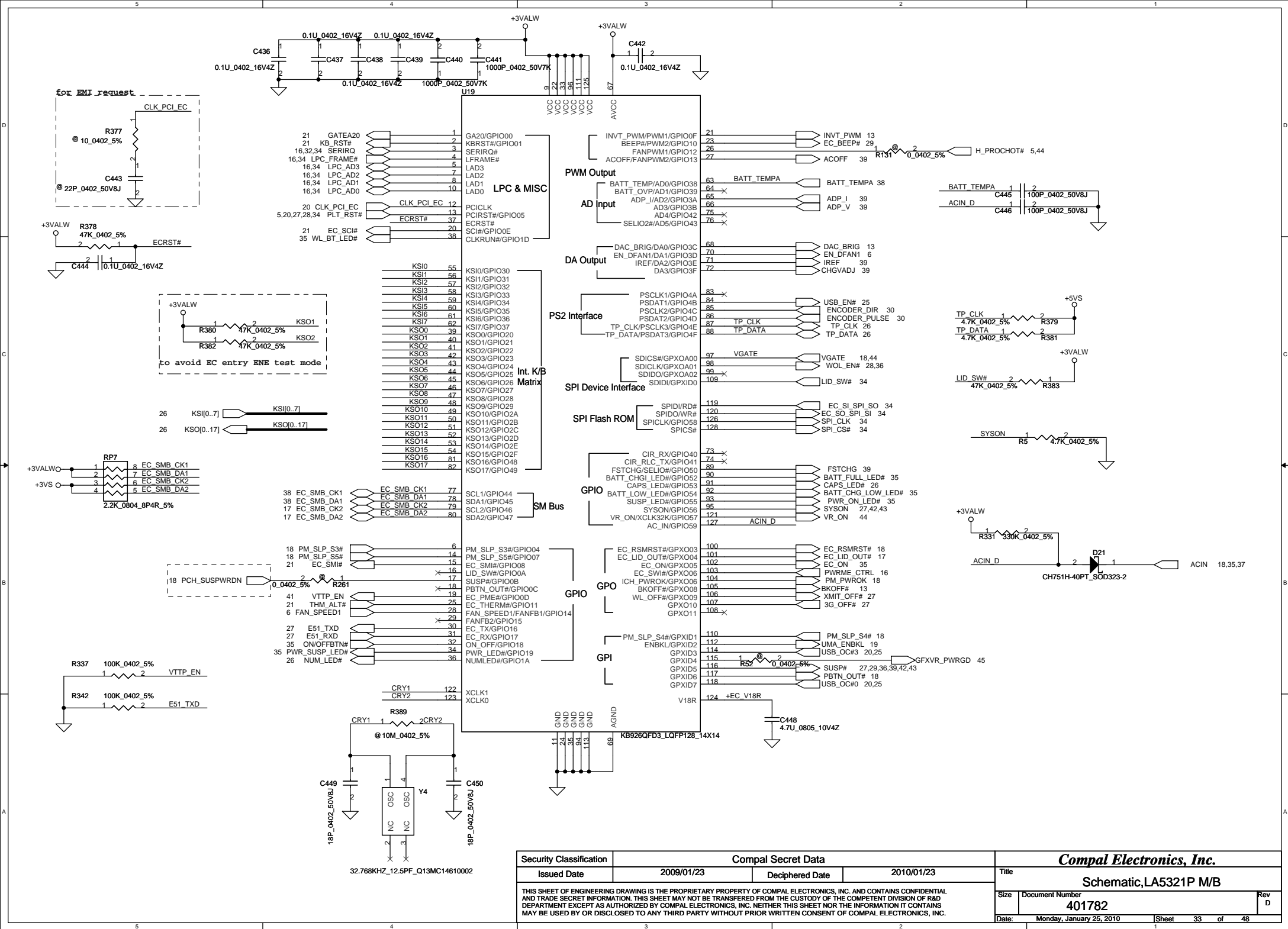
THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.
IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE
PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE
REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO
SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.
THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

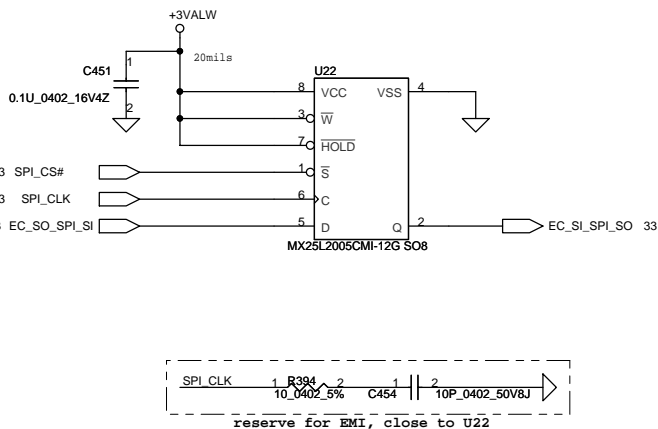
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.



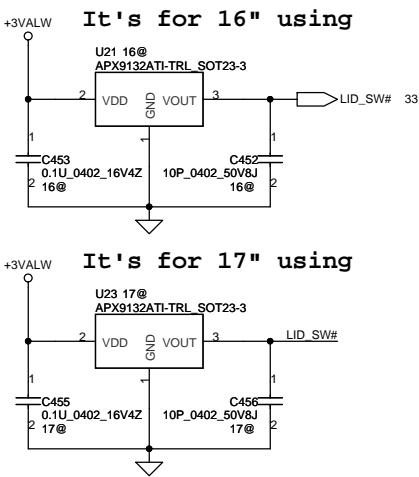
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				Size	Document Number	Rev D
				Custom	401782	
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SPI Flash (256KB)

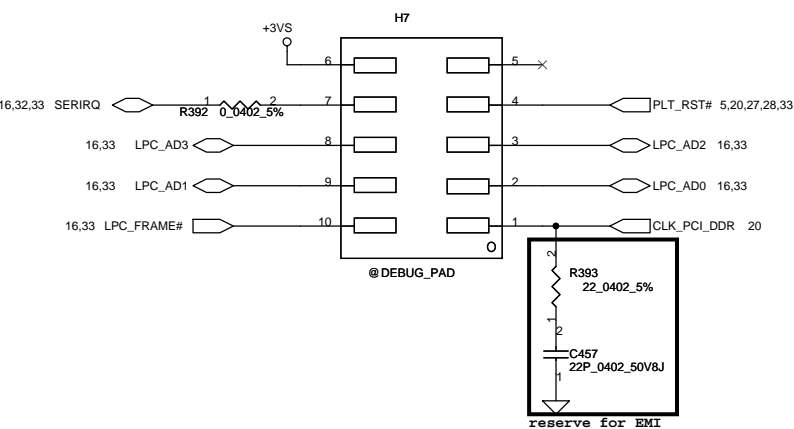


Lid SW



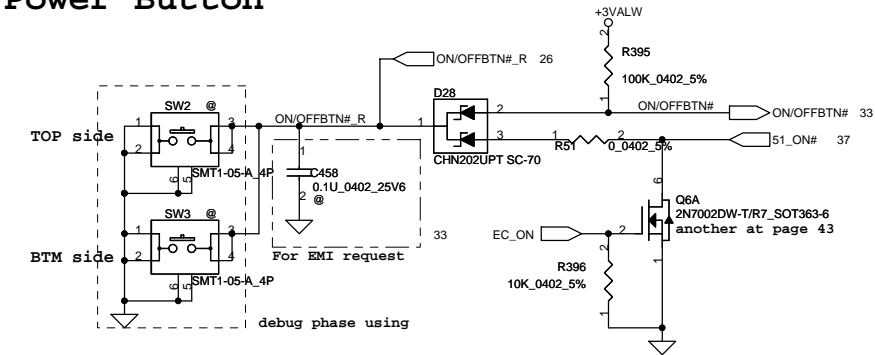
LPC Debug Port

Please place the PAD under DDR DIMM.

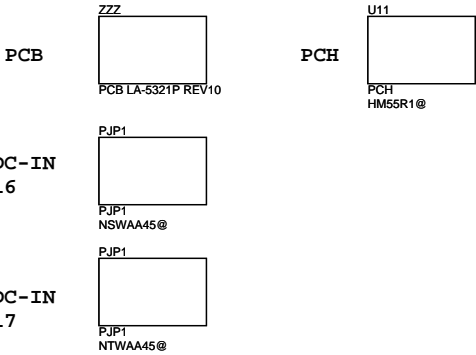


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Power Button

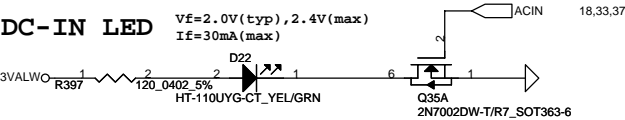


ISPD

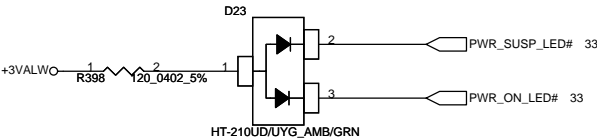


DC-IN LED

Vf=2.0V(typ), 2.4V(max)
If=30mA(max)

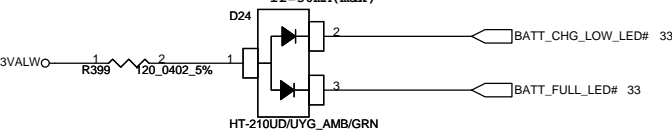


POWER/SUSPEND LED

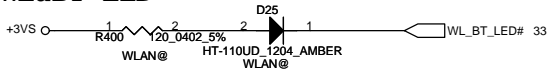


BATT CHARGE/FULL LED

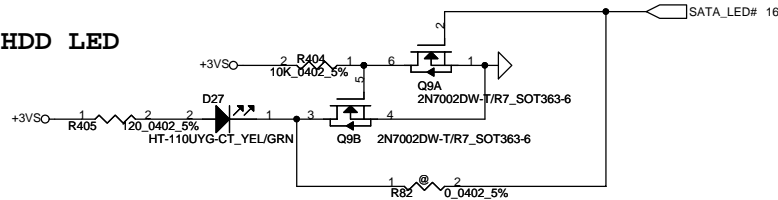
Vf=1.9V(typ), 2.4V(max) for amber
Vf=2.0V(typ), 2.4V(max) for green
If=30mA(max)



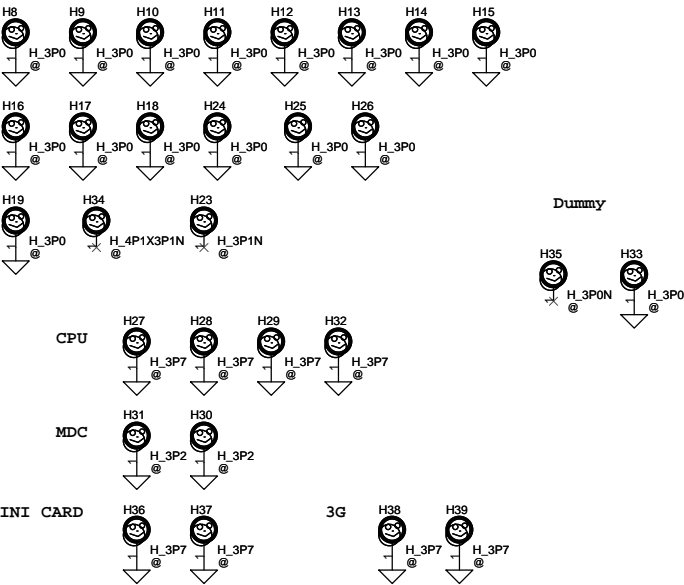
WL&BT LED



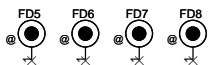
HDD LED



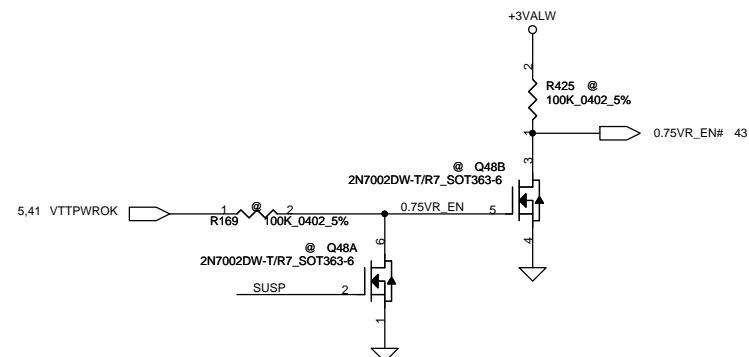
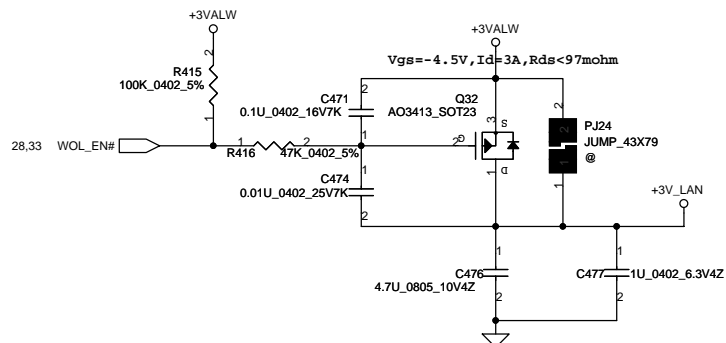
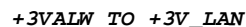
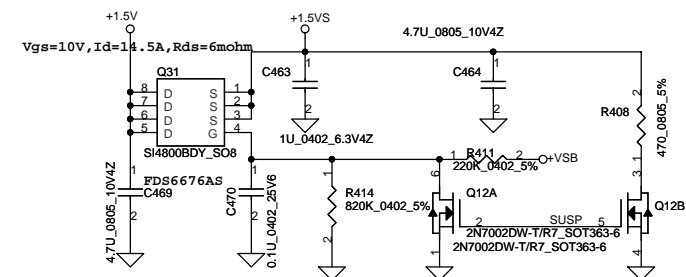
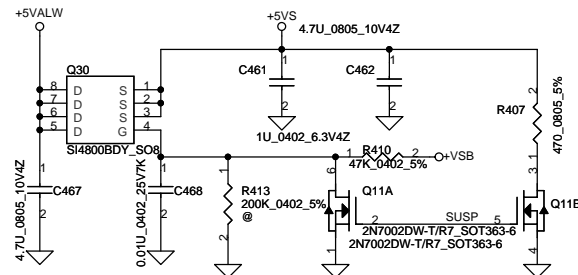
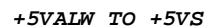
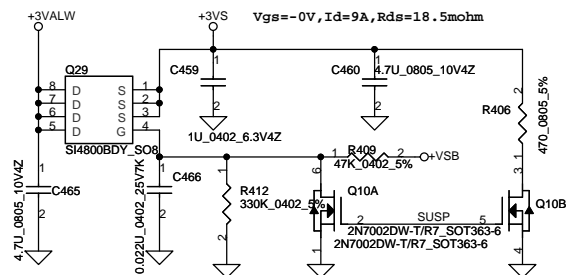
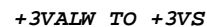
Screw Hole



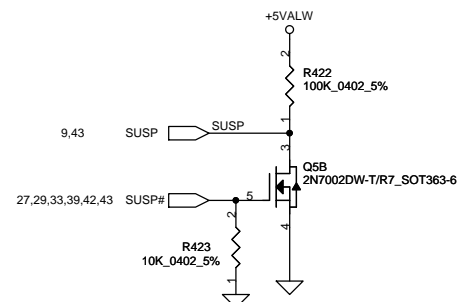
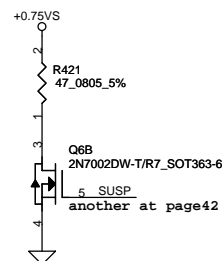
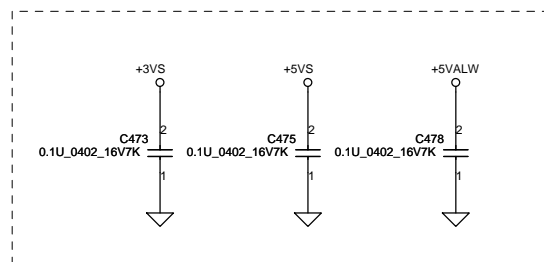
PCB Federal Mark PAD



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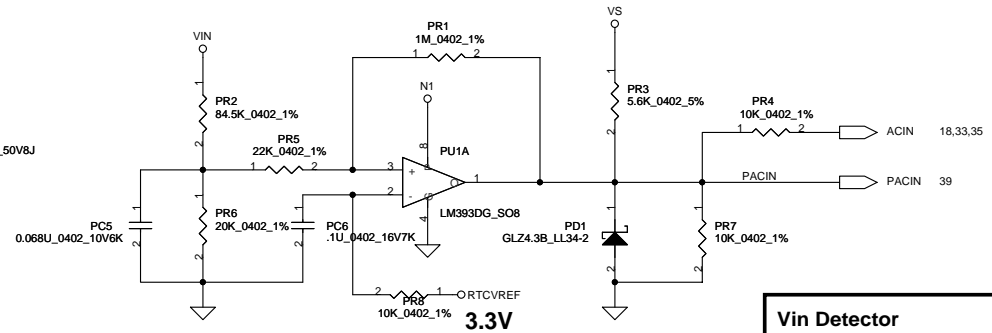
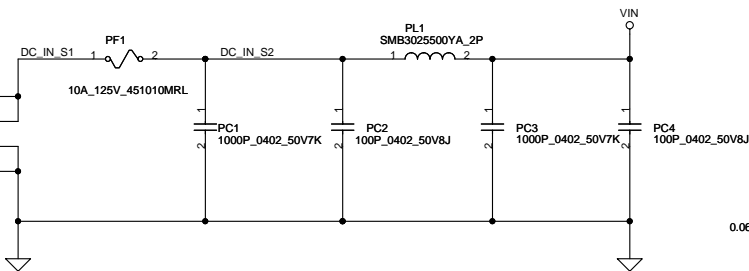


Reserve for EMI test



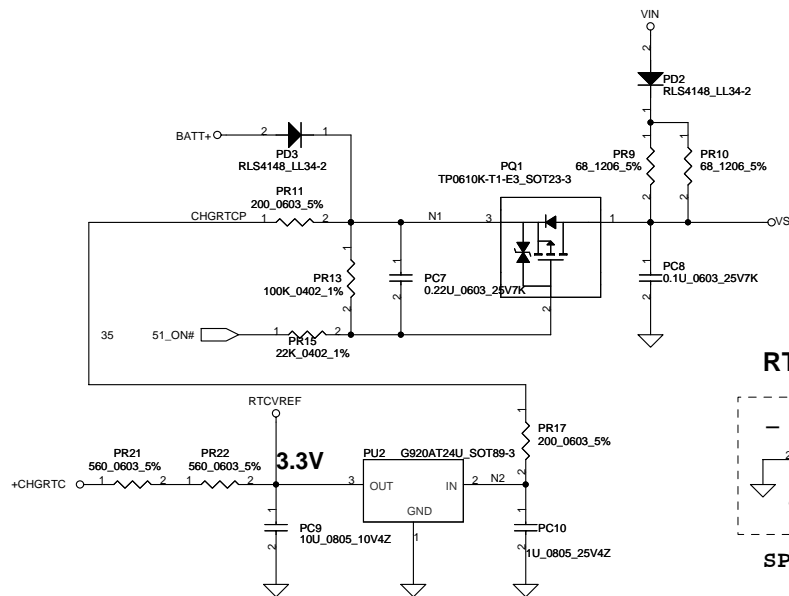
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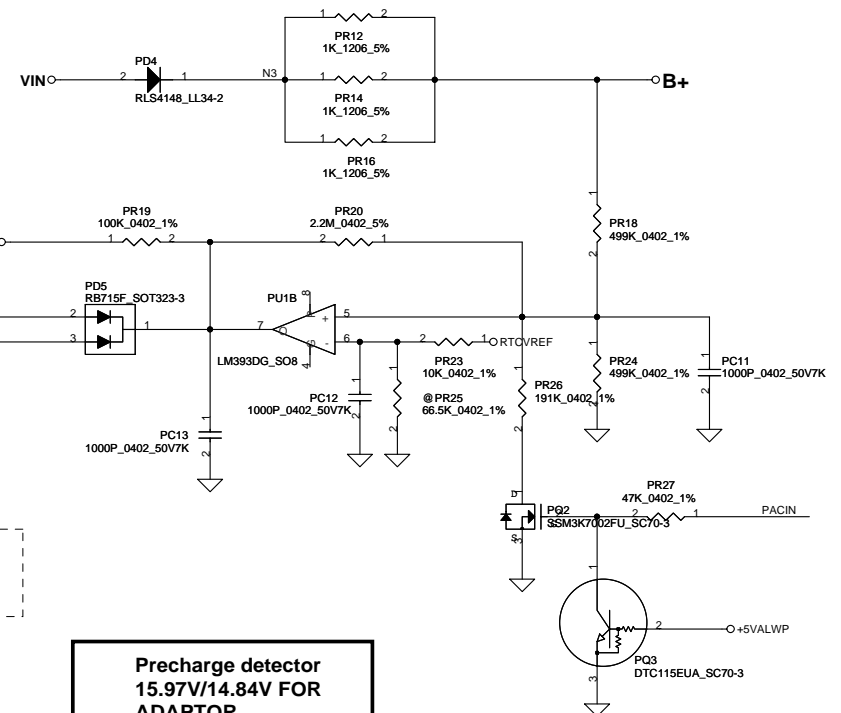
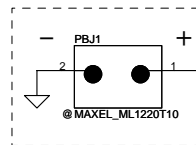


Vin Detector

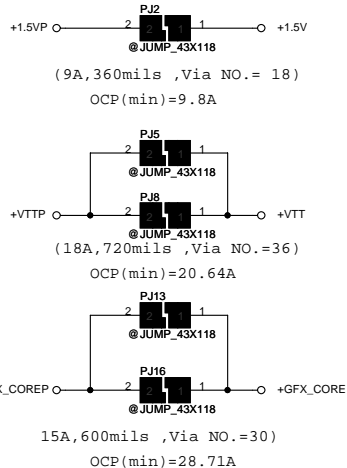
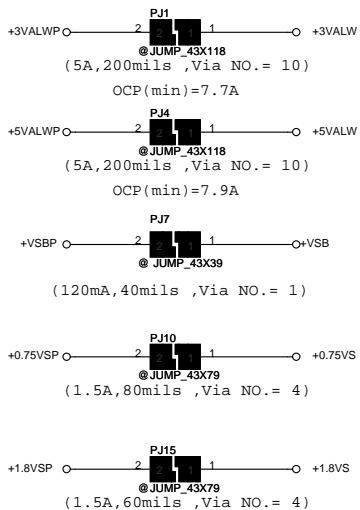
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



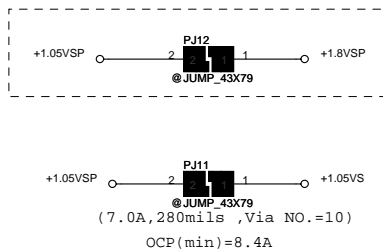
RTC Battery



Precharge detector 15.97V/14.84V FOR ADAPTOR



Add on 10/29

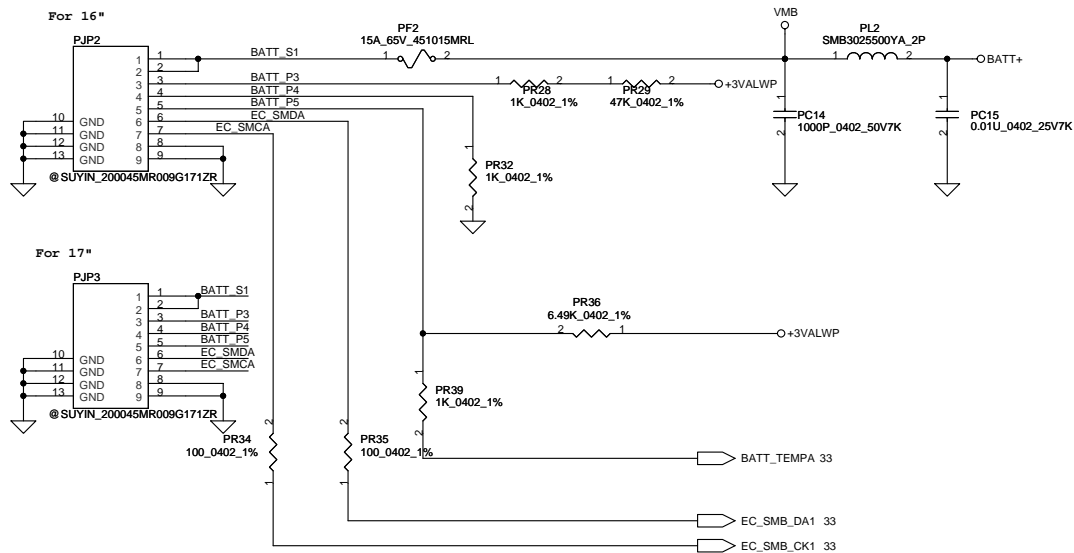


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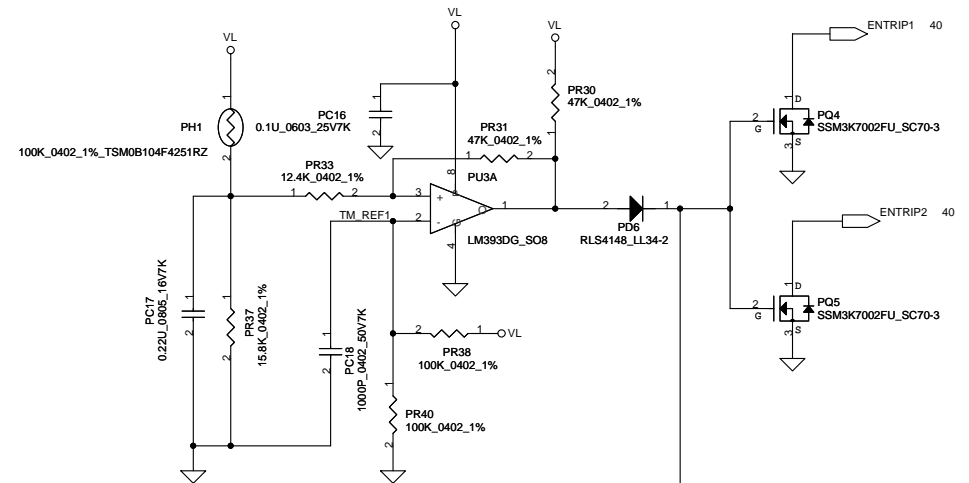
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Schematic,LA5321P M/B

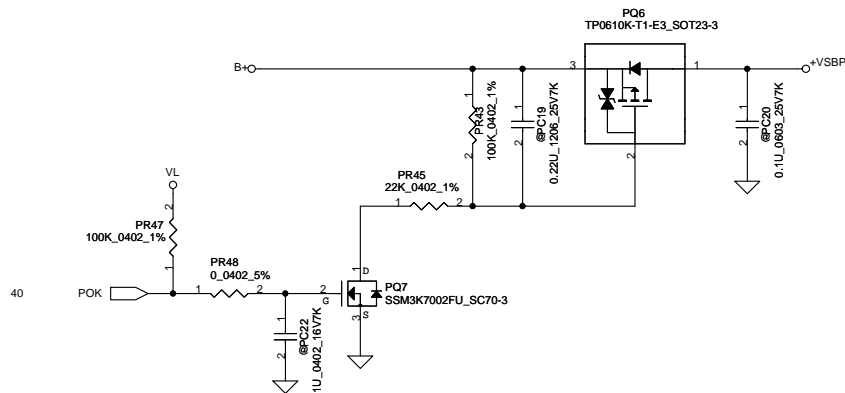
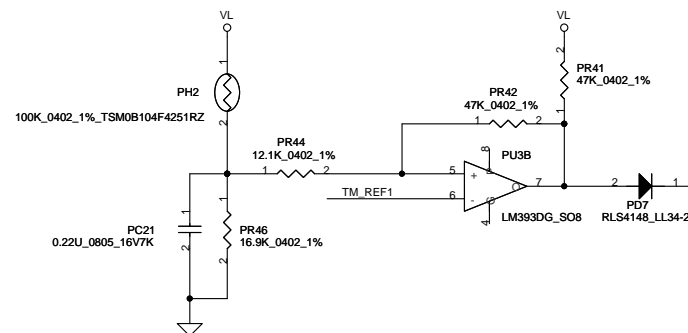
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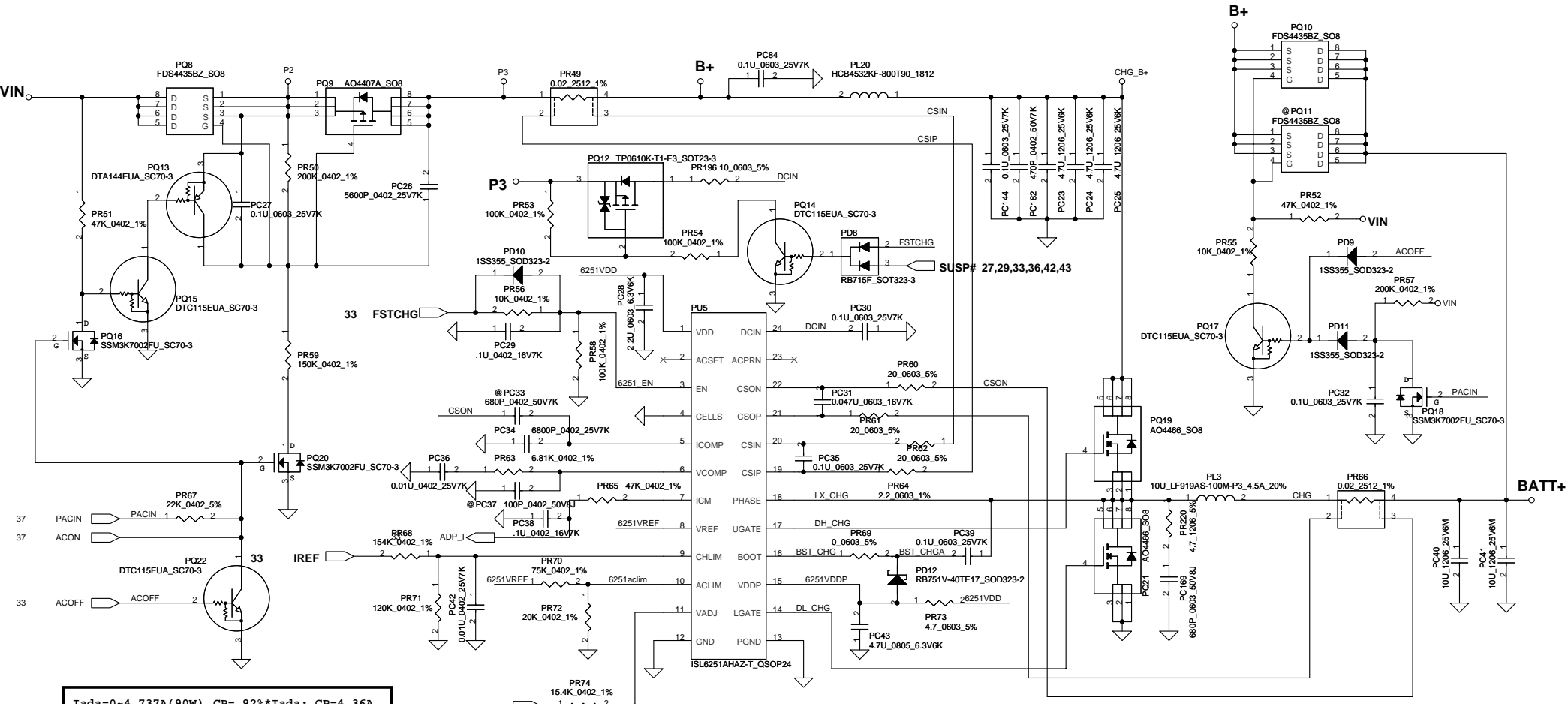
PH1 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 90 degree C
 Recovery at 55 degree C



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Iada=0~4.737A(90W) CP= 92%*Iada; CP=4.36A

Iada=0~3.42A(65W) CP= 92%*Iada; CP=3.147A

CP mode

Vaclim=0.736V(90W) PR70=53.6k PR49=0.015

Vaclim=1.08V(65W) PR70=75k PR49=0.02

CC=0.25A-3A

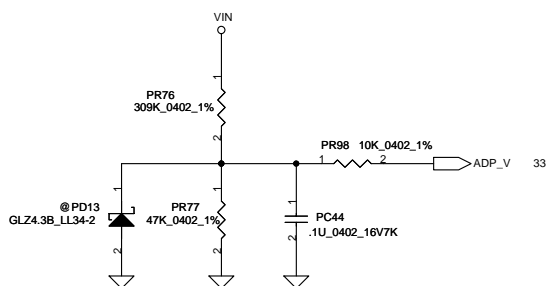
IREF=1.016*Icharge

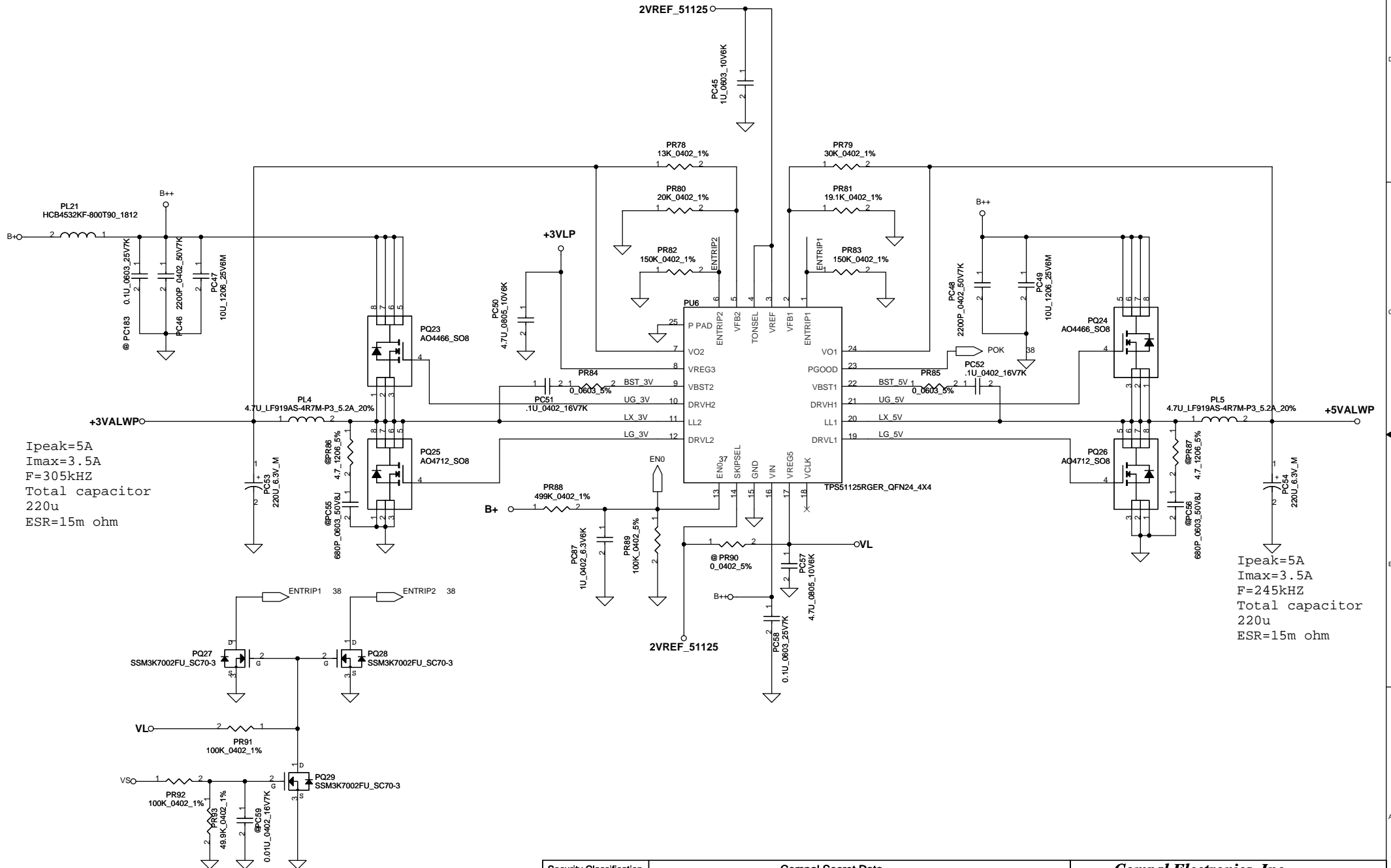
IREF=0.254V~3.048V

VCHLIM need over 95mV

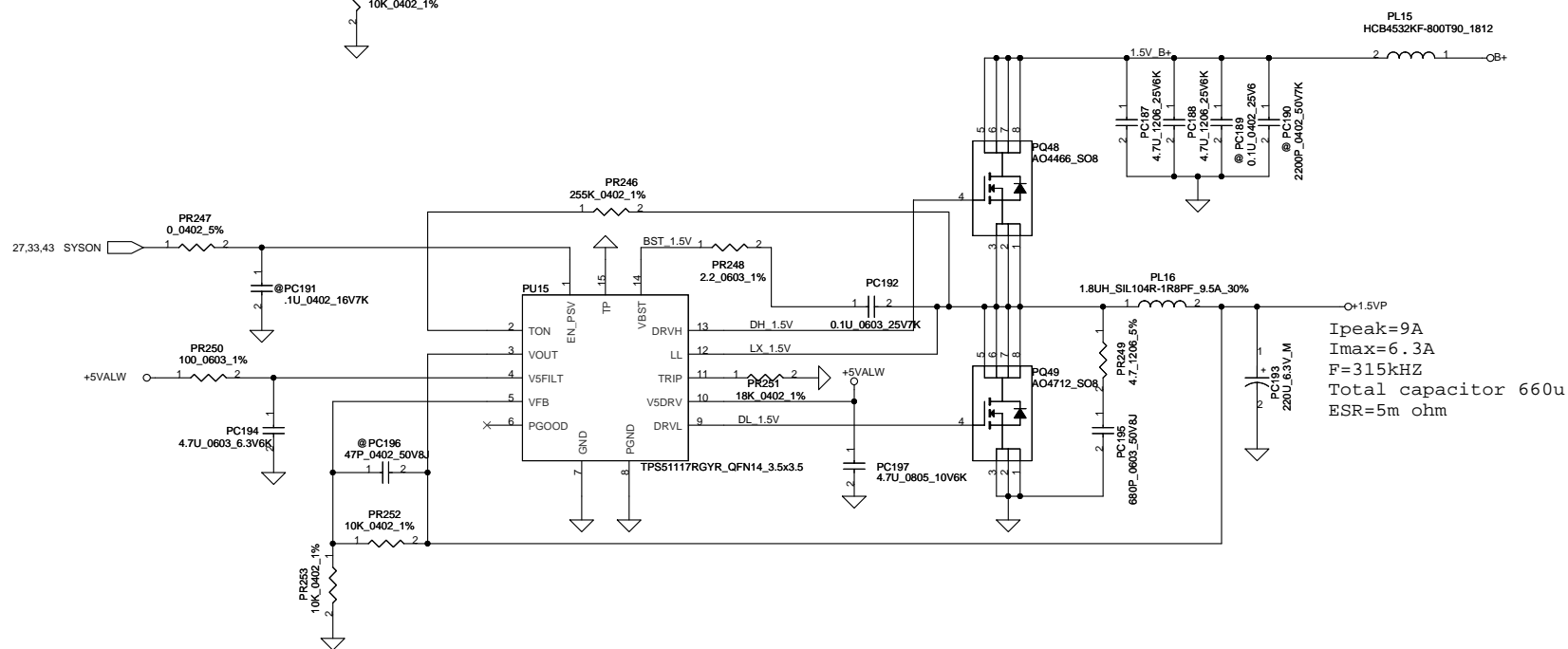
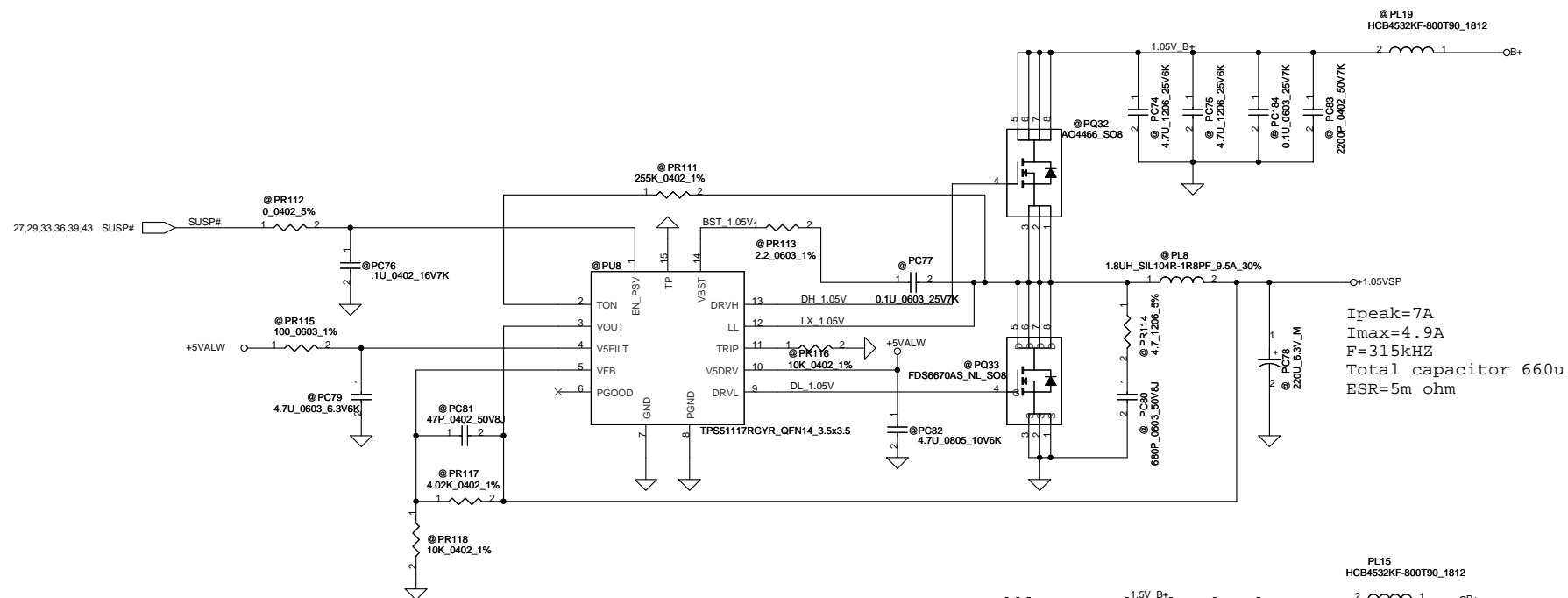
CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CELLS	VDD	GND	Float
CELL number	4	3	2

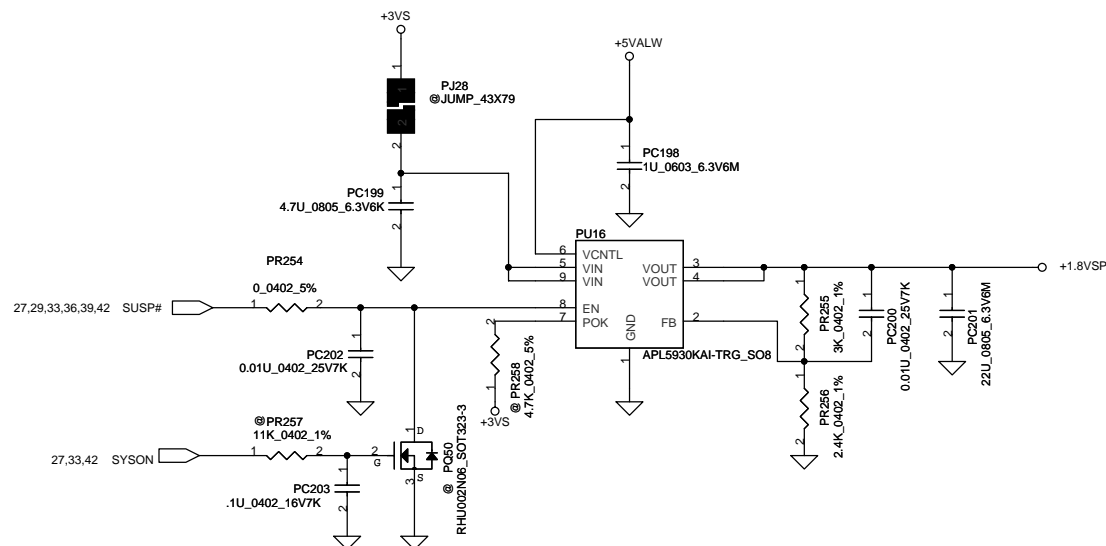
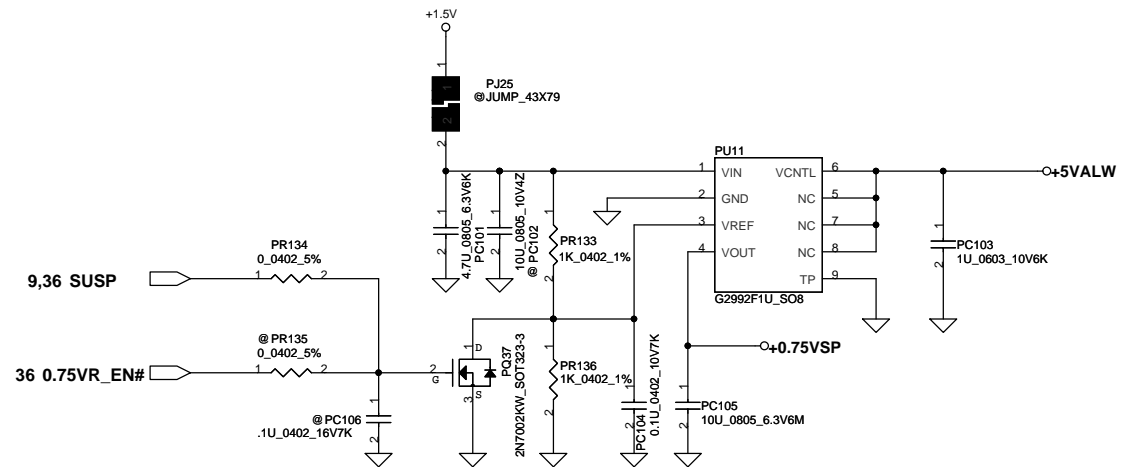




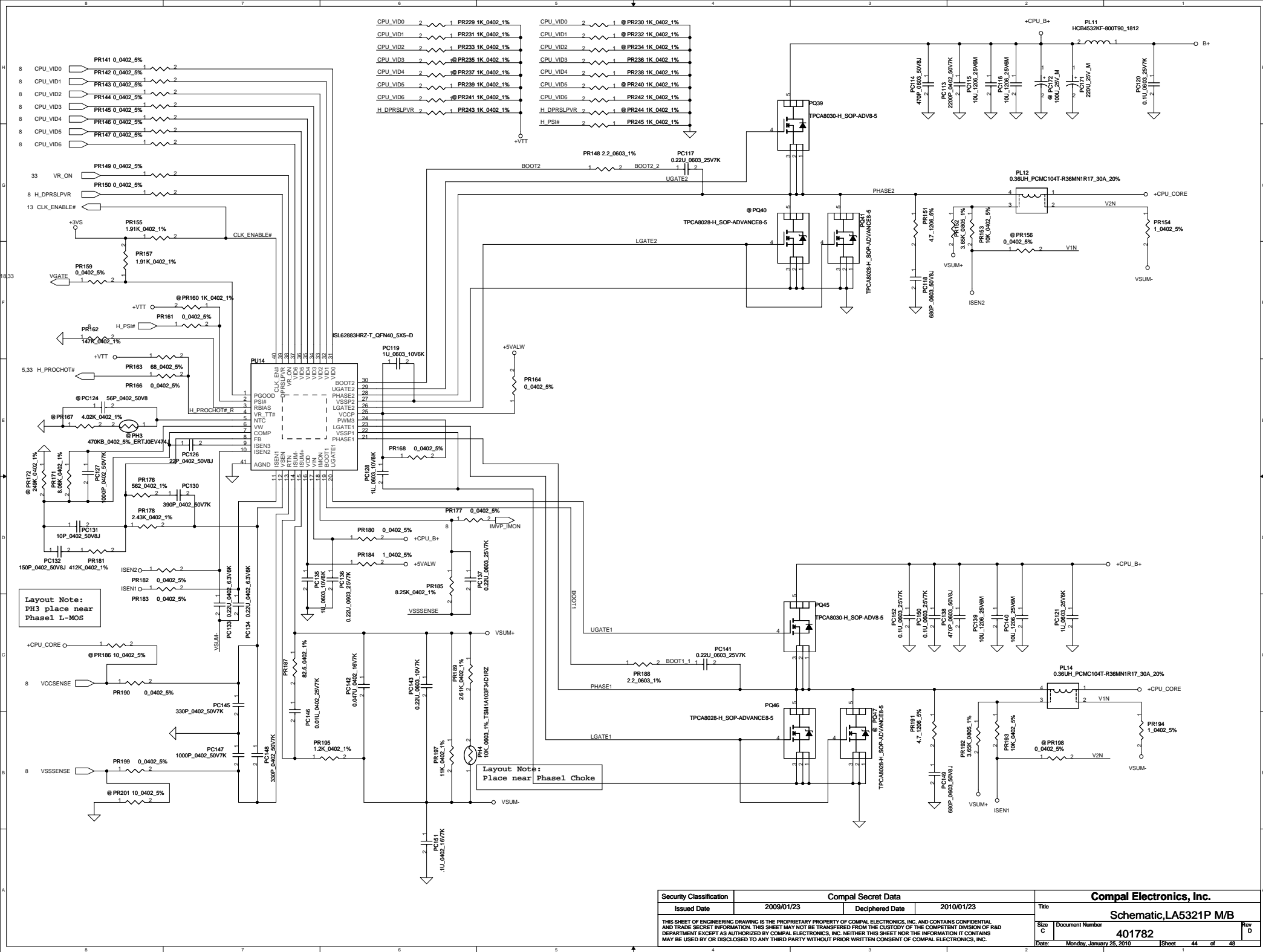
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PIR (Product Improve Record)

NSWAA LA-5321P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
6/29	18		Change R324 from 10K to 330K	To solve ACIN LED issue
7/02	21		Change BT_PWR# from GPIO0 to GPIO34, add VGA_HDMI_HPD on GPIO0.	For common design with NSKAA
7/02	26		DEL JCAM (R431,R432,C403,R371,R373,R374,R375,L20)	CAM cable combine with LVDS
7/02	13		DEL R387	Remove +5VALW power to camera
7/02	31		DEL YC1,CC10,CC12	Remove 12MHz crystal to cardreader
7/02	31		DEL RC2	Remove +3VALW to cardreader
7/03	13		Add R126,R401	Reserve +1.5VS to clk gen for low power clk gen test
7/03	13,21		Add R155	Reserve LVDS_SEL on PCH GPIO45
7/03	16,33		Connect PCH GPIO33 to EC pin 103 as PWRME_CTRL Change 3G_OFF# from EC pin 103 to pin 107	To reflash ME BIOS
7/17	35		Add R82 on SATA_LED#	Reserve for cost down plan
7/17	20		DEL R277,D12, Connect USB_OC#3_D to USB_OC#3	
7/17	18,33,35		DEL R384, D14. Add R331	Modify ACIN circuit
7/17	13,35		Change Q7,Q34 to Dual Q35	For cost down
7/17	15		DEL R169~R172, C267,C268,C271,C272	No need for ASMedia level shifter
7/20	5,9,11,21		Add Q41,R19,R127,R22,D54,U16,R33,R84,Q33,R424,R418, C267,Q46,C472,R417,C230,C218,C205,C186,PJ30,PJ31,R83 Q48,R425,R169 Add RST_GATE on PCH GPIO46	Reserve S3 power reduction circuit
7/27	33		Add R5	To solve SYSON glitch issue
7/27	21,33		Connect PCH GPIO49 to EC pin25 as THM_ALT#	Reserve for test
7/27	8,9,11		Add C159,C160,C271,C180,C179,C185,C217,C268	For cost down
7/30	36		Add C473,C475,C478	For EMI request
7/30	16,34		Change U13 to 8MB, U22 to 1MB	For SW and EC request
7/30	20		DEL Braidwood circuit	Calpella don't support Braidwood

NSWAA LA-5321P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
8/4	5		Change VTTPWROK to VTTPWROK_CPU on CPU side	Modify S3 power saving circuit
8/4	15		Add R189 on PCH_HDMI_HPD	Add for no IHDMI sku
8/4	36		Change Q31 from SI4856 to SI4800	Cost down
8/19	15		Change HDMI level shifter from ST to ASMedia	For better HDMI signal quality
8/19	13,19		Add R128,R130 for PCH BKL control	Reserve for deep green test

NSWAA LA-5321P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
9/28	32		Change UB1 pin53 connection from PCI_SERR# to SERIRQ	Modify PCMCIA circuit
9/28	16		Change C287,C290 from 18p to 15p	To fine tune RTC timing
10/15	15,21		Connect PCH_HDMI_HPD to PCH GPIO0	For TVAP HDMI control
10/28	5		Reserve C301,C384,C389	Reserve for S3 power saving circuit

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P47-PWR_CHARGER	Change PR65 4.7 to 47k	For CPU throttling setting (2009/06/05)
EVT		P47-PWR_CHARGER	Change PR70 8.25k to 24k	Set 75W CP (2009/06/05)
			Change PR72 26.7k to 20k	
			Change PR49 0.015 Ohmto 0.02 Ohm	
EVT		P47-PWR_CHARGER	Change PQ8,PQ9,PQ10 A04407 to FDS4435	Change PMOS for UMA SKU (2009/06/05)
EVT		P43-PWR_1.05VSP/1.5VP	Change PR115,PR250 422 Ohm to 100 Ohm	Avoid 2nd source RT8209B can no power on (2009/06/05)
			Change PC79,PC194 1U to 4.7U	
EVT		P43-PWR_1.05VSP/1.5VP	Change PR116 14.7k to 10k	Set 1.05V OCP to 8.54A(2009/06/05)
			Change PR251 13.7k to 18k	Set 1.5V OCP to 9.98A(2009/06/05)
EVT		P42-PWR_VTTP	Change PR99 5.9k to 2.43k	Set VTT OCP to 19.7A(2009/06/05)
DVT		P46-PWR_GM VGA_CORE	Change PC218 15P to 100P	Correct link error (2009/07/07)
DVT		P46-PWR_GM VGA_CORE	Change PC211 SE080224K80 to SE000005Z80	Change voltage rating 10V to 25V (2009/07/07)
DVT		P45-PWR_CPU_CORE	PC133, PC134 SE083224Z80 to SE124224K80	PC133, PC134 tolerance Y5V to X5R(2009/0/07)
DVT		P49-PWR_VTTP	Change PR99 2.43k to 4.99k	Set OCP(2009/07/07)
DVT		P43-PWR_1.05VSP/1.5VP	Change PC79, PC194 SE00000MAN0 to SE107475K80	Change part number(2009/07/07)
DVT		P41-PWR_3VALWP/5VALWP	Add PC87 1U_0402_6.3V6K	Avoid pre-charge can not finish(2009/07/07)
DVT		P41-PWR_3VALWP/5VALWP	Add PC45 0.22U to 1U	Prevent +3VALW/+5VALW can't boot up (2009/07/07)
DVT		P45-PWR_CPU_CORE	Change PR229-PR245 and PR160 10k to 1k	Change VID, PSI# and DPRSLPVR select resistor from 10k to 1k (2009/07/17)
DVT		P45-PWR_CPU_CORE	Change PR157 10k to 1.91k	Change PGOOD pull high resistor 10k to 1.91k(2009/07/17)
DVT		P45-PWR_CPU_CORE	Remove PH3, PC124, PR167	Modify circuit for CPU_CORE(2009/07/17)
			Change PC133, PC134 pin 2 from GND to VSUM-	
			Change PR152, PR192 0402 size to 0805 size	
DVT		P46-PWR_GM VGA_CORE	Remove PR281, PC227	Modify circuit for GFX (2009/07/17)
DVT		P39-PWR_BATTERY CONN / OTP	Change +3VLP to +3VALWP	Remove +3VLP power rail (2009/07/17)
DVT		P42-PWR_VTTP	Remove PR290, PR291, PR292, PR293, PR293,PR105, PC228, PC229, PQ53, PQ54	Remove VTT voltage switch circuit (2009/07/17)
DVT		P47-PWR_CHARGER	Change PC84 0.1U	For EMI solution(2009/07/23)
DVT		P47-PWR_CHARGER	Add PC144 0.1U,Add PC182 470P	For EMI solution(2009/07/23)
DVT		P47-PWR_CHARGER	Add PC144 0.1U,Add PC182 470P	For EMI solution(2009/07/23)
DVT		P42-PWR_VTTP	Add PC230 0.1U	For EMI solution(2009/07/23)
DVT		P42-PWR_VTTP	Add PR100 4.7U, PC70 680P	Add snubber(2009/07/23)
DVT		P42-PWR_VTTP	Change PR95 0 ohm to 2.2 ohm	Add boot strap resistor (2009/07/23)
DVT		P42-PWR_VTTP	Change PR94 3.4k to 1.5k, PR101 1k to 3k	For HW solution(S3 power reduction)(2009/07/23)
DVT		P42-PWR_VTTP	Add PU14	For power test(2009/07/23)
DVT		P52-PWR_0.75VSP/1.1VSP	Add 0.75VR_EN# control signal	For HW solution(S3 power reduction) (2009/07/23)
DVT		P45-PWR_CPU_CORE	Change PR148, PR188 0 to 2.2 ohm	Add boot strap resistor(2009/07/23)
DVT		P45-PWR_CPU_CORE	Add PR151, PR191 4.7 ohm, PC118, PC149 680P	Add snubber(2009/07/23)
DVT		P45-PWR_CPU_CORE	Add PC114, PC138 470P	For EMI solution(2009/07/23)
DVT		P45-PWR_CPU_CORE	Add PC120 0.1U	For EMI solution(2009/07/23)
DVT		P45-PWR_CPU_CORE	Add PC121 1U	For EMI solution(2009/07/23)
DVT		P46-PWR_GM VGA_CORE	Change PL18 SH00000AC00 to SH05056BM00	Change current rating to 25A(2009/07/27)
DVT		P47-PWR_CHARGER	Change PQ9 FDS4435 to A04407A	For design change(2009/07/27)
DVT		P45-PWR_CPU_CORE	Remove PQ40, PQ47	For design change(2009/07/28)
DVT		P52-PWR_0.75VSP/1.1VSP	Change PC101 10U to 4.7U	For design change(2009/07/28)
DVT		P52-PWR_0.75VSP/1.1VSP	Change PC106 SE076104KM8 to SE076104K80	Change to COMPAL PN(2009/08/03)
DVT		P45-PWR_CPU_CORE	Change PC151 SE076104KM8 to SE076104K80	Change to COMPAL PN(2009/08/03)
DVT			Change PC53, PC54, PC78, PC193 SF22001M200 to SF000001H00	SF22001M200 is forbids to use (2009/08/03)
DVT		P45-PWR_CPU_CORE	Change PR178 2.43k to 2.26k	Change Rdroop for load line (2009/08/03)
DVT		P42-PWR_VTTP	Change PU7 ISL6268 to APW7138	For cost down (2009/08/03)
			Remove PC71 0.01U	For APW7138 solution (2009/08/03)
DVT		P39-PWR_BATTERY CONN / OTP	Change PR33 13.7k to 12.4k	Set OTP (2009/08/03)
			Change PR37 15.4k to 15.8k	
DVT		P46-PWR_GM VGA_CORE	Change PC223 SE071150J1M to SE071150J80	Change PC223 to COMPAL PN (2009/08/03)
DVT		P47-PWR_CHARGER	Add PR220 4.7 ohm, PC169 680P	Add charger snubber(RF solution) (2009/08/03)
DVT		P45-PWR_CPU_CORE	Add PC113 2200P	RF solution (2009/08/03)
PVT		P47-PWR_CHARGER	Change PR70 24k to 75k	Set 65W CP (2009/09/04)
PVT		P42-PWR_VTTP	Change PL7 0.47U to 1U	Design change (2009/09/04)
PVT		P45-PWR_CPU_CORE	Change PR178 2.26k to 2.37k	Change Rdrrap for load line (2009/09/04)
PVT		P45-PWR_CPU_CORE	Add PC150, PC152 0.1U (SE042104K80)	For EMI soltion (2009/09/14)
PVT		P45-PWR_CPU_CORE	Add PC121 1U	For EMI soltion (2009/09/14)
PVT		P42-PWR_VTTP	Add PC85, PC186 0.1U	For EMI soltion (2009/09/14)
PVT		P42-PWR_VTTP	Remove PC66, PC68 10U	Design change (2009/09/14)
PVT		P47-PWR_CHARGER	Change PR64 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P42-PWR_VTTP	Change PR95 PN SD013220B80 to SD014220B80	Use same PN (2009/09/14)
PVT		P43-PWR_1.05VSP/1.5VP	Change PR113, PR248 0 ohm to 2.2 ohm	Add boot trap resistor(2009/09/14)
			Add PR114, PR249 4.7 ohm, PC80, PC195 680P	Add snubberr(2009/09/14)
PVT		P45-PWR_CPU_CORE	Change PR148, PR188 PN to SD014220B80	Use same PN(2009/09/14)
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PVT		P42-PWR_1.05VSP/1.5VP	Change	PR117 8.25k to 4.02k	Avoid FB trace noise (2009/09/18)
			Change	PR118, PR252, PR253 20.5k to 10k	
PREMP		P45-PWR_DCIN/DECTOR	Change	PC7 SE041224K80 to SE000005Z80	Change CAP size from 1206 to 0603 (2009/10/09)
PREMP		P46-PWR_BATTERY CONN / OTP	Change	PR44 13.7k to 12.1k	Modify OTP setting (2009/10/09)
PREMP		P44-PWR_CPU_CORE	Change	PR178 2.37k to 2.43k	Change CPU_CORE OCP 52A to 57A and modify load line (2009/10/09)
			Change	PR195 1.1k to 1.2k	
PREMP		P44-PWR_CPU_CORE	Change	PC121 SE000009R80 to SE000006900	Change HW part to power part PN (2009/10/09)
PREMP		P44-PWR_CPU_CORE	Change	PL12, PL14 SH000005680 to SH12036BM00	Use 5% tolerance DCR choke (2009/10/09)
PREMP		P41-PWR_VTTP	Change	PR94 1.5k to 39.2k	Adjust VTTPWROK voltage 3.3V to 1.05V (2009/10/27)
			Change	PR101 3k to 10.5k	
PREMP		P42-PWR_1.05VSP/1.5VP	Remove	1.05V components	Cost down (2009/11/03)
MP		P41-PWR_VTTP	Change	PR94 39.2k to 6.81k	Modify resistor for VTTPWROK voltage (2009/11/26)
			Change	PR101 10.5k to 2k	